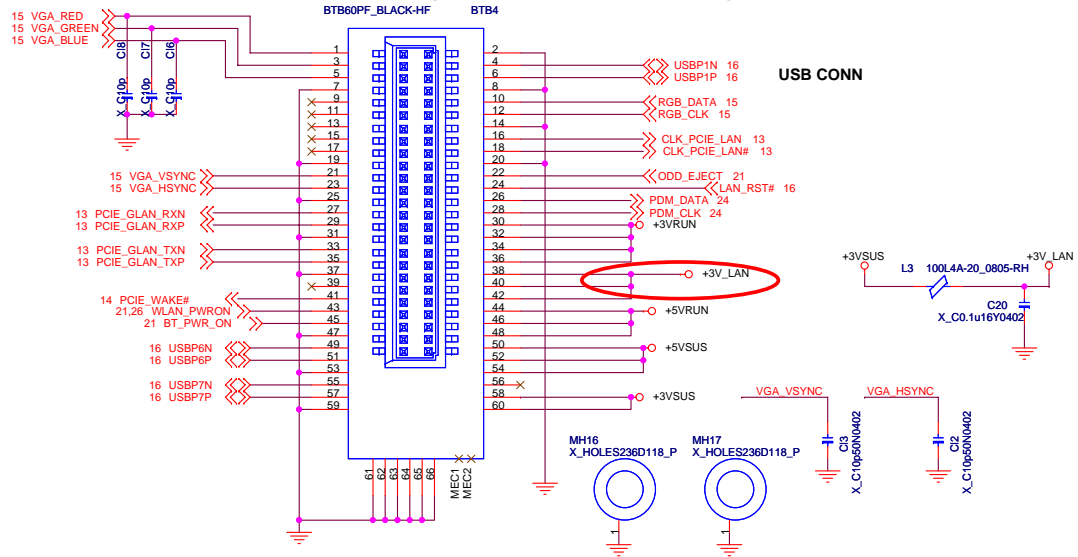
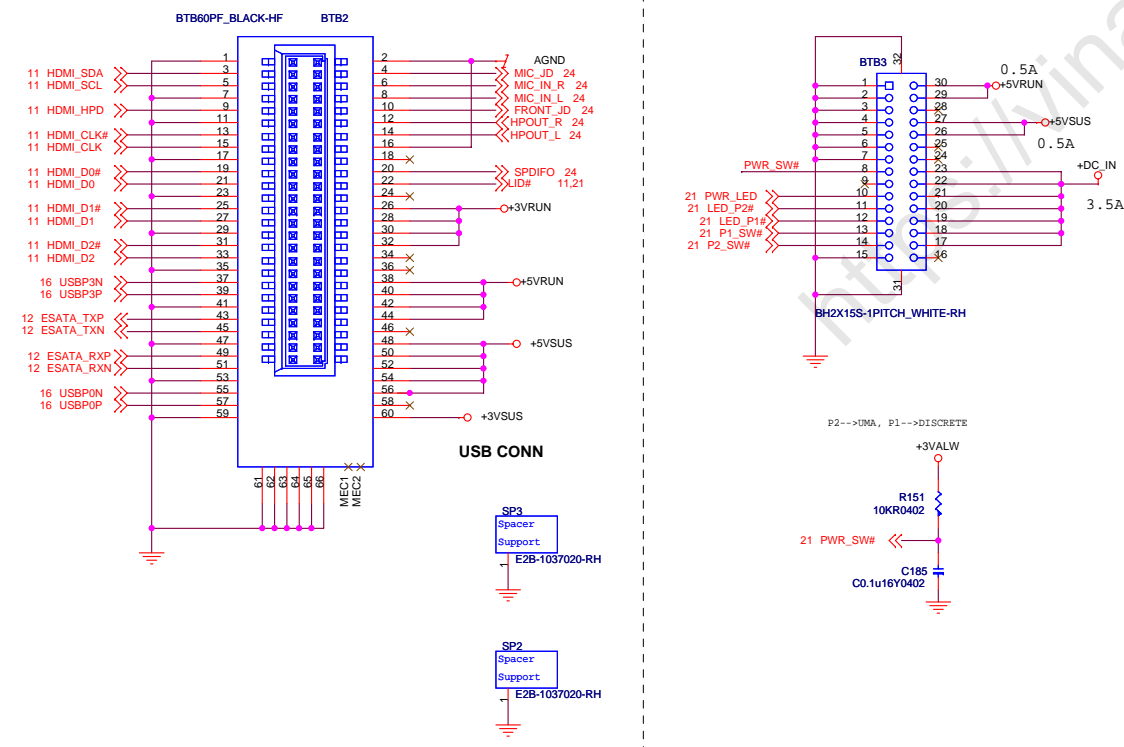


- 
- CPU**  
Auburndale 2 Core  
or  
Clarksfield 4 Core  
Page 3-8
- PCH**  
Page 12-20
- DDR-SODIMM0**  
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- DDR-SODIMM1**  
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Page 23
- ODD**  
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- e-SATA**  
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- USB 1/2/0**
- Cardreader**  
UB6250  
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RTL8111D  
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Conn. X2  
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- Audio Codec**  
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- SPI Flash**  
32M  
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- KBC**  
ENE 3926  
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- TP & KB**  
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- Smart Fan**  
CPU & System
- SPI BIOS**  
Page 21
- DC JACK & Selector**
- SYS POWER**
- +3V +5V**  
TPS51125
- +1.5V DIMM**  
TPS51117
- +VT(1.05V)**  
TPS51117
- CPU POWER**  
ISL62882HRZ-T
- CHARGER**  
MAX17005ETP+
- +1.8V RUN**  
APL5912KAC
- +VCC\_GFXCORE**  
ISL62881HRZ-T
- USB 0 : Standard USB Connector**  
**USB 1 : Standard USB Connector**  
**USB 2 : Mini\_PCIE slot**  
**USB 3 : ESATA Connector**  
**USB 4 : Camera**  
**USB 5 : CardReader**  
**USB 6 : BT and WLAN slot**  
**USB 7 : BT and WLAN slot**  
**USB 8 : Finger Print**  
**USB 9 : Mini\_PCIE slot**
- CLK GEN**  
IDT3199  
Page 22
- 14MHZ CRYSTAL**
- MSI** MICRO-STAR INT'L CO.,  
File **BLOCK DIAGRAM**

## 60PIN BTB I/O Connector(VGA, USB1, LAN,BT)



## 60PIN BTB I/O Con (HDMI,Audio,ESATA),ARRAY,USB) 30PIN BTB I/O Conn(AC IN LID,Power Switch)



MSI CORPORATION				
Title	HDD, CON, MINI_PCIE			
Size	Document Number	<RevCode>		Rev
Customer	MS-16D3			0A
Date:	Tue Jul 22 2010	Sheet	27	of 43

1. 2010.01.28 by leozhang
  - a. Base on summer's SCH to add ME mylar which would be located SD/MMC connecter (MYLAR16)
2. 2010.01.29 by leozhang
  - a. Base on 0129 SCH to modify PC81's assembly level.
3. 2010.02.01 by leozhang
  - a. Base on 0129 SCH to add ME's mylar (Mylar 17)
4. 2010.02.23 by leozhang
  - a. Base on 0201 SCH to remove G-senser
5. 2010.03.02 by leozhang
  - a. Base on 0223 SCH to remove JNC17,JNC18 for power components
  - b. Base on 0223 SCH to add R244 and C150 for webcam power on issue.
  - c. Modify footprint of PC69,PC70,PC99,PC74,PC72,PC73,PC75 and remove PC28,PC40,PC100,PC103,PC96,PC107 for power noise issue

Title		
<Title>		
Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, March 03, 2010	Sheet 1 of 1

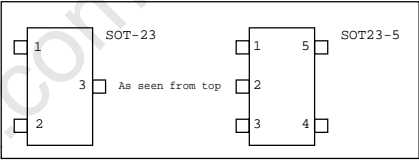
SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails			
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	12V	S0, (S3-S5)	
+5VALW	5V	S0, (S3-S5)	
+5VRUN	5V	S0, S3	
+5VSUS	5V	S0	
+3VALW	3.3V	S0, (S3-S5)	
+3VRUN_CK505	3.3V	S0	Clock, MCH
+3VSUS	3.3V	S0, S3	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0, (S3-S4)	DDR core
+1_5VSUS	1.5V	S0	
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDR command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	GMCH Graphics core rail

Net Naming Conventions

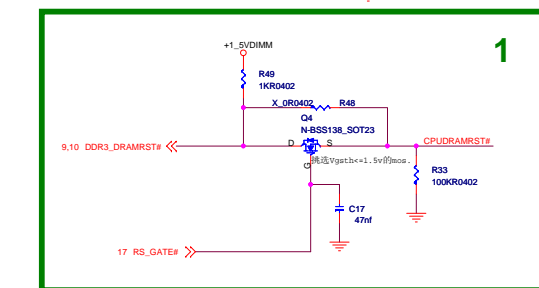
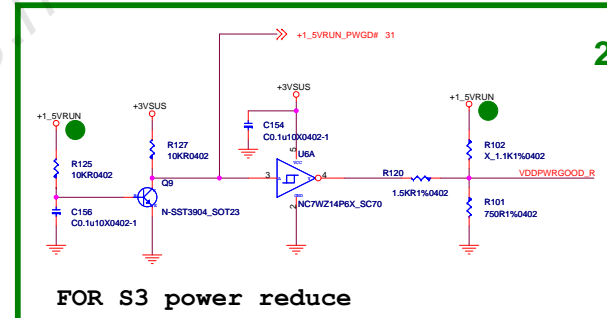
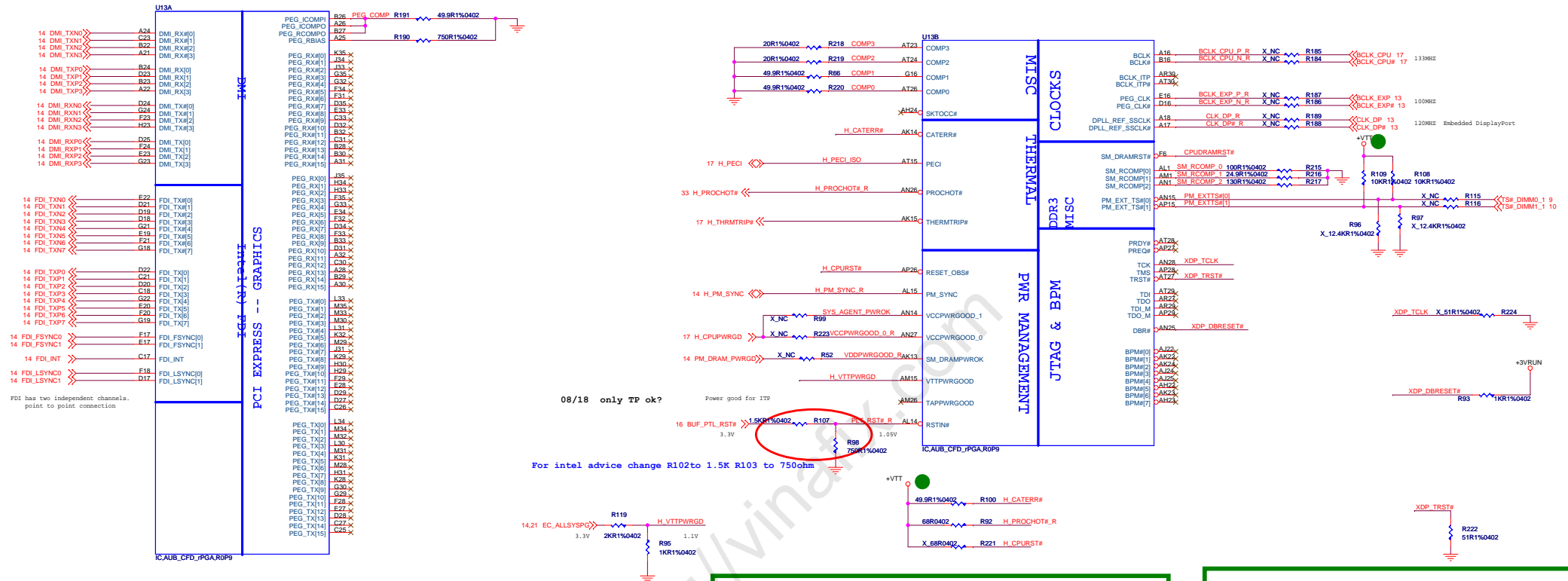
Suffix
# = Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



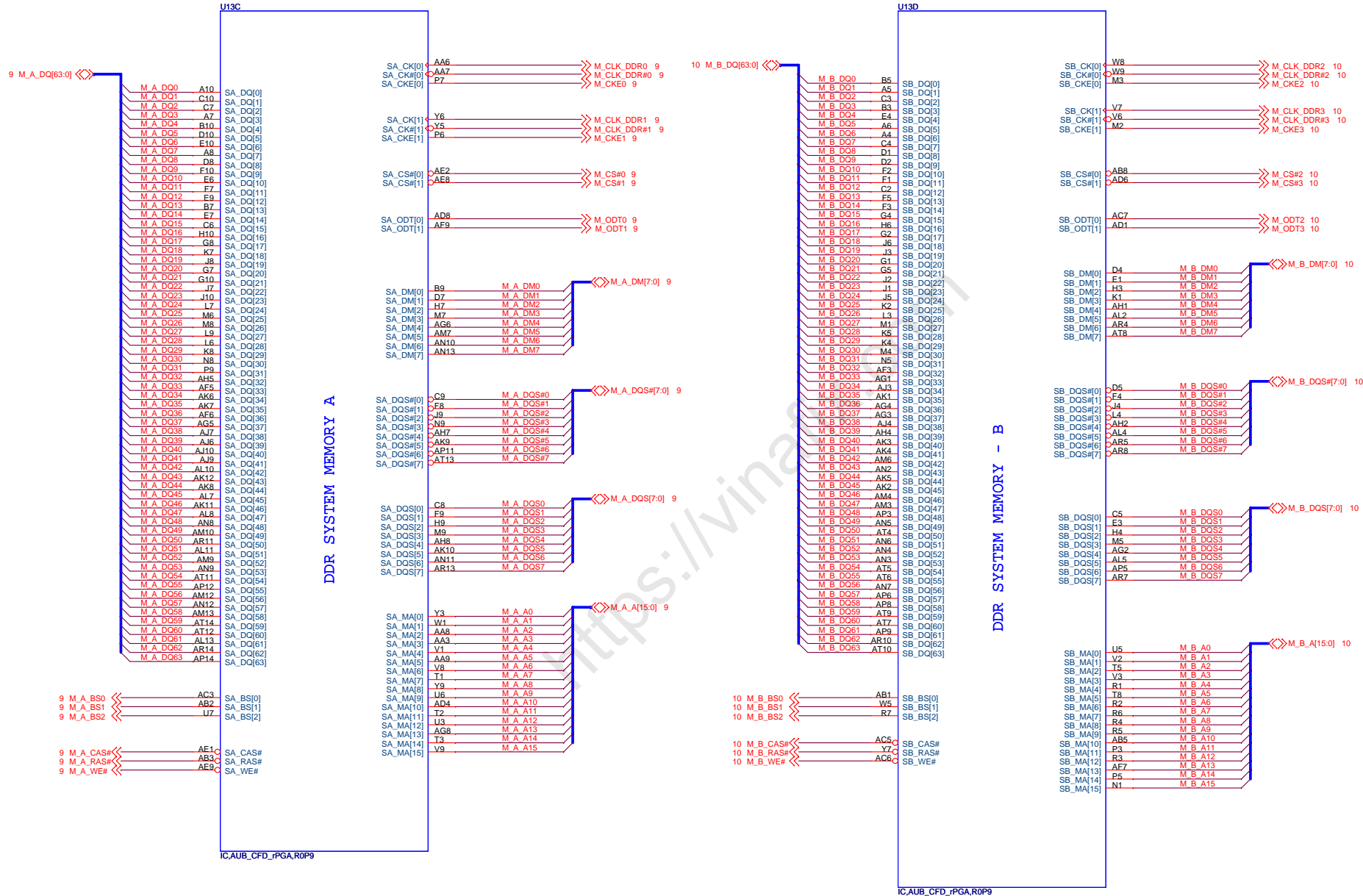
Power States	SLP S3#	SLP S4#	SLP S5#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF	OFF

# AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



FOR S3 power reduce

# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



# AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

## PROCESSOR CORE POWER

IccMax: 5V=48A, 1V=35A, ULV=27A

AG35	VCC1
AG34	VTT0_2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VTT0_12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U34	VCC71
U33	VCC72
U32	VCC73
U31	VCC74
U30	VCC75
U29	VCC76
U28	VCC77
U27	VCC78
U26	VCC79
R34	VCC80
R33	VCC81
R32	VCC82
R31	VCC83
R30	VCC84
R29	VCC85
R28	VCC86
R27	VCC87
R26	VCC88
P34	VCC89
P33	VCC90
P32	VCC91
P31	VCC92
P30	VCC93
P29	VCC94
P28	VCC95
P27	VCC96
P26	VCC97
	VCC98
	VCC99
	VCC100

IC\_AUB\_CFD\_PGA\_R0P9

1.1V RAIL POWER

CPU CORE SUPPLY

POWER  
CPU VIDS

SENSE LINES

IccMax\_VTT: 5V=18A, 1V=16A, ULV=16A

VTT0_1	AH14
VTT0_2	AH12
VTT0_3	AH11
VTT0_4	AH10
VTT0_5	J14
VTT0_6	J13
VTT0_7	H14
VTT0_8	H12
VTT0_9	G14
VTT0_10	G12
VTT0_11	G11
VTT0_12	F13
VTT0_13	F14
VTT0_14	F12
VTT0_15	F11
VTT0_16	E14
VTT0_17	E12
VTT0_18	D14
VTT0_19	D13
VTT0_20	D12
VTT0_21	D11
VTT0_22	C14
VTT0_23	C13
VTT0_24	C12
VTT0_25	C11
VTT0_26	B14
VTT0_27	B12
VTT0_28	A14
VTT0_29	A13
VTT0_30	A12
VTT0_31	A11

VTT0_33	AF10
VTT0_34	AE10
VTT0_35	AC10
VTT0_36	AB10
VTT0_37	Y10
VTT0_38	W10
VTT0_39	U10
VTT0_40	T10
VTT0_41	J12
VTT0_42	J11
VTT0_43	J16
VTT0_44	J15

PSIW	AN33	PSIW 33
VID[0]	AK35	H_VID0 33
VID[1]	AK33	H_VID1 33
VID[2]	AK34	H_VID2 33
VID[3]	AL35	H_VID3 33
VID[4]	AL33	H_VID4 33
VID[5]	AM33	H_VID5 33
VID[6]	AM35	H_VID6 33
PROC_DPRSPLVR	AM34	PM_DPRSPLVR R
		X NC R94
		PM_DPRSPLVR 33

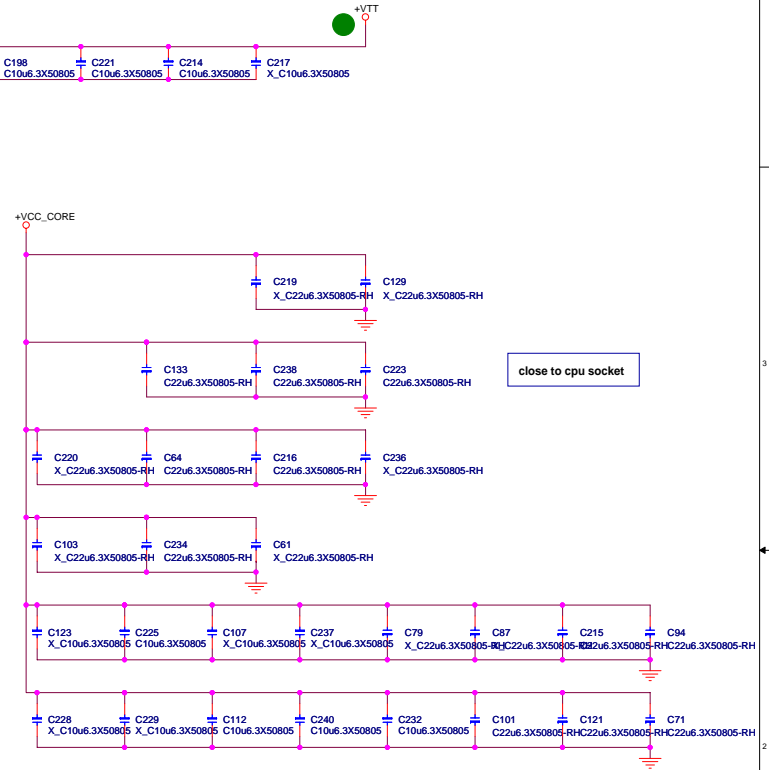
VTT\_SELECT G15 X

VTT rail voltage for Auburndale/Arrandale is 1.05 V and for Clarksfield is 1.1 V.

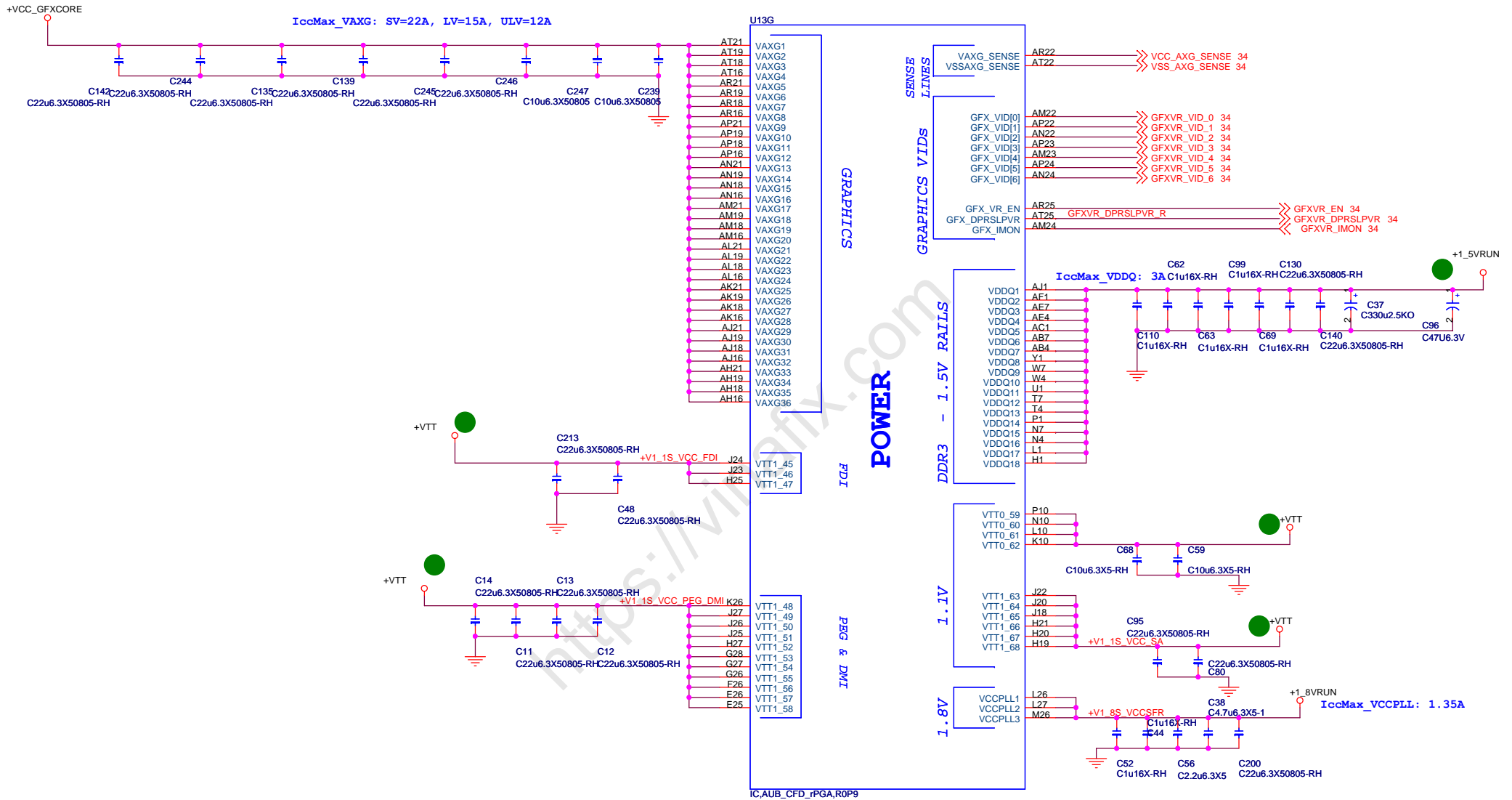
ISENSE	AN35	IMVP_IMON 33
VCC_SENSE	AJ34	VCCSENSE R
VSS_SENSE	AJ35	VSSSENSE R
		VCCSENSE 33
		VSSSENSE 33
VTT_SENSE	B15	VTT_SENSE 32
VSS_SENSE_VTT	A15 X	

TP60:  
1:Chk1st:Connect VSS\_SENSE\_VTT to GND. (Need to confirm)  
2:CRB:TP  
ukimao1008

## PROCESSOR CORE POWER

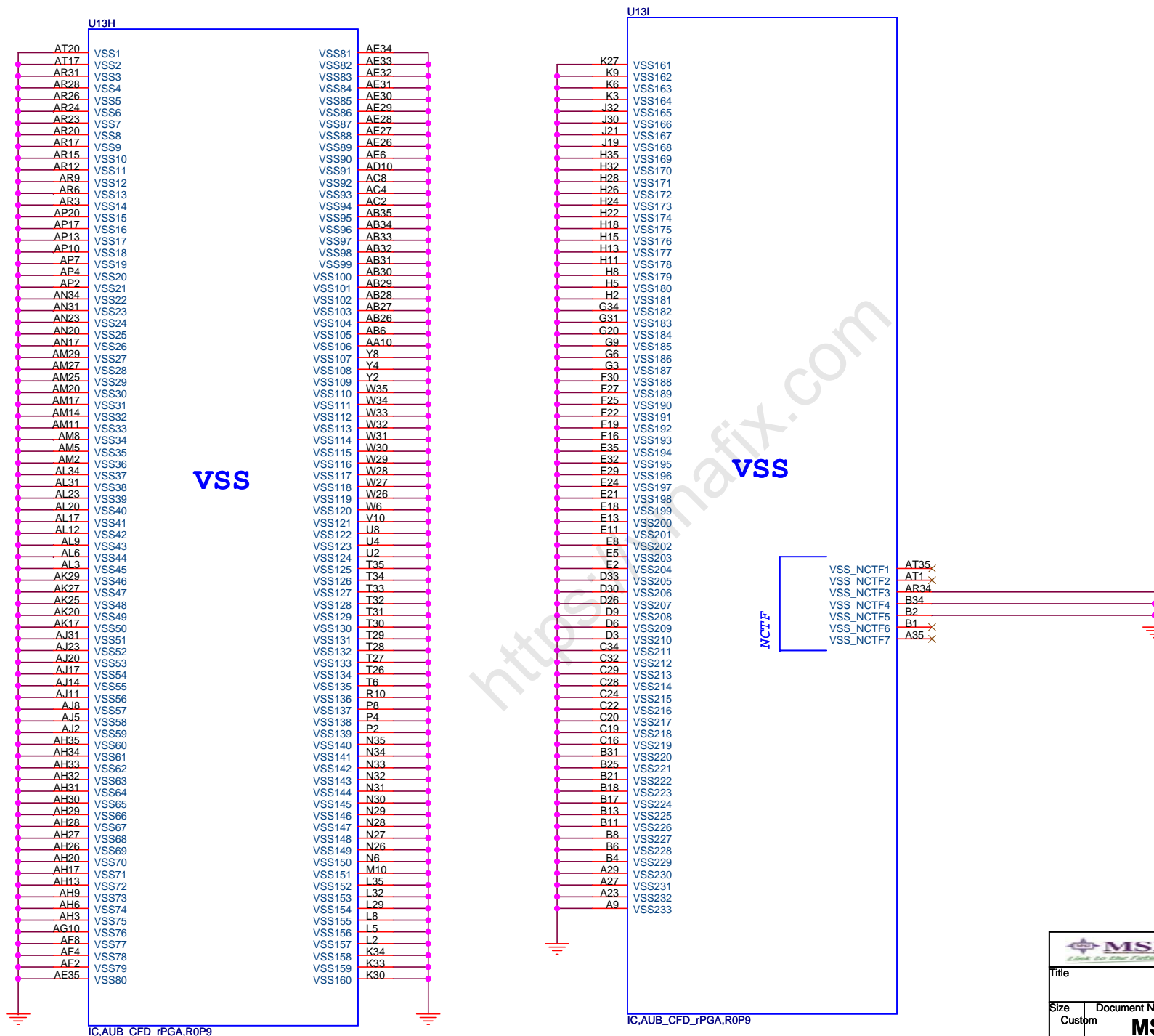


AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

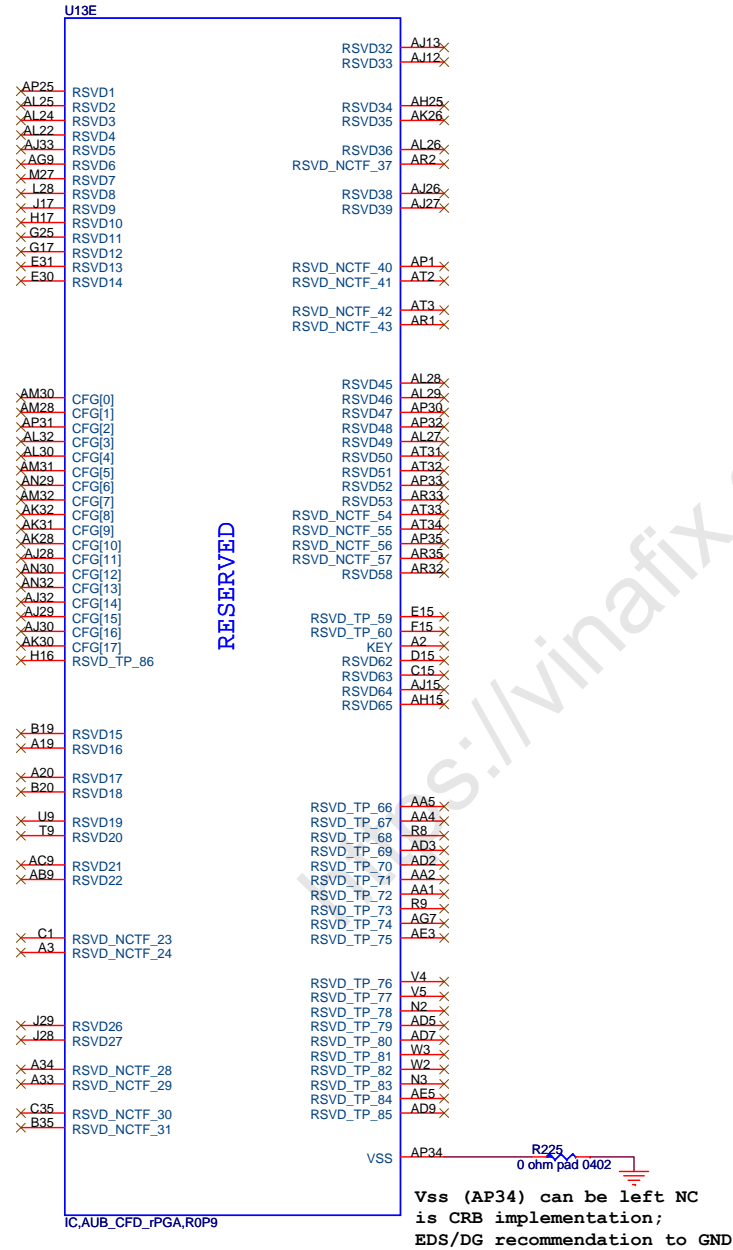




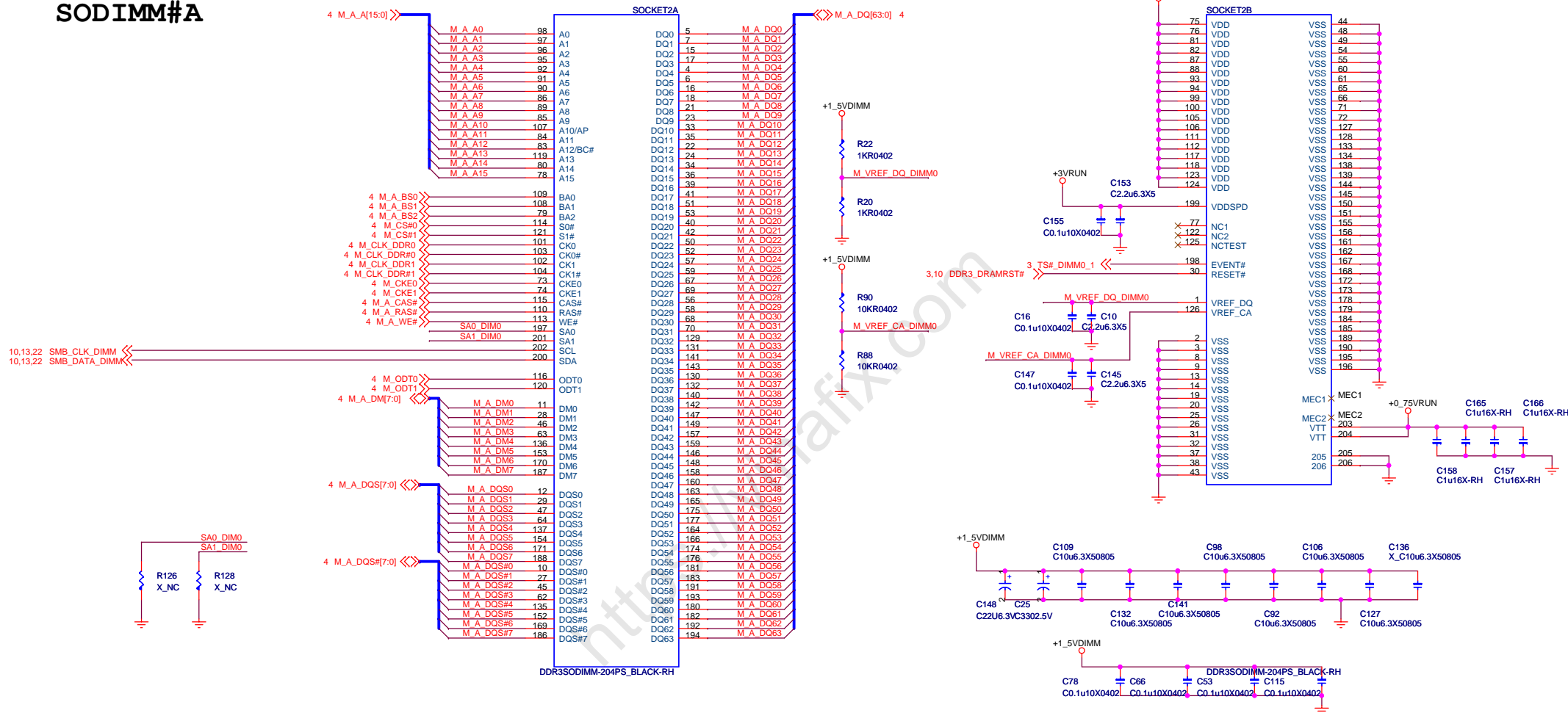
# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



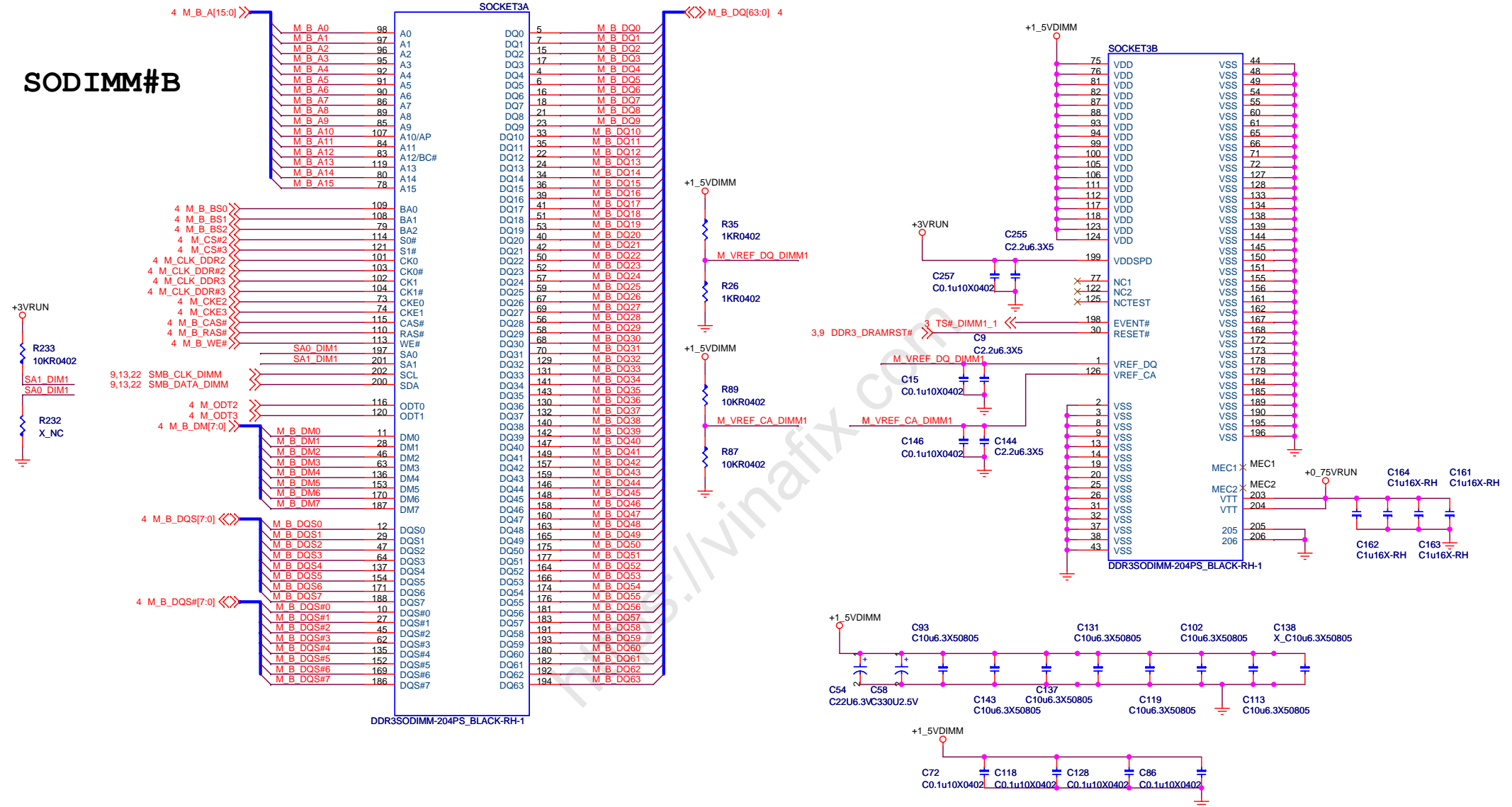
# AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED)



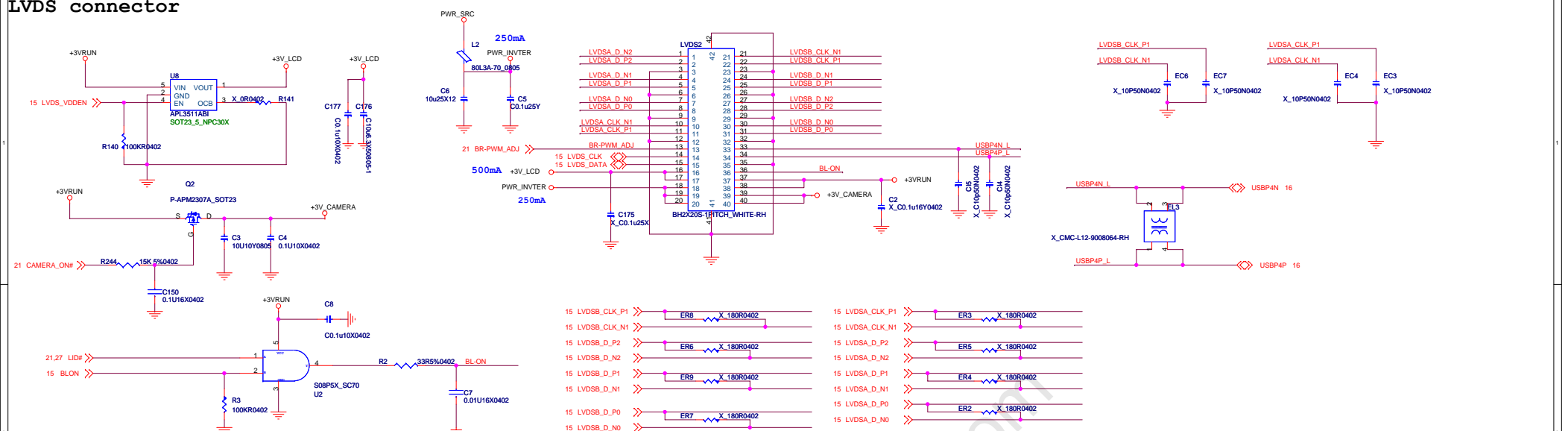
**SODIMM#A**



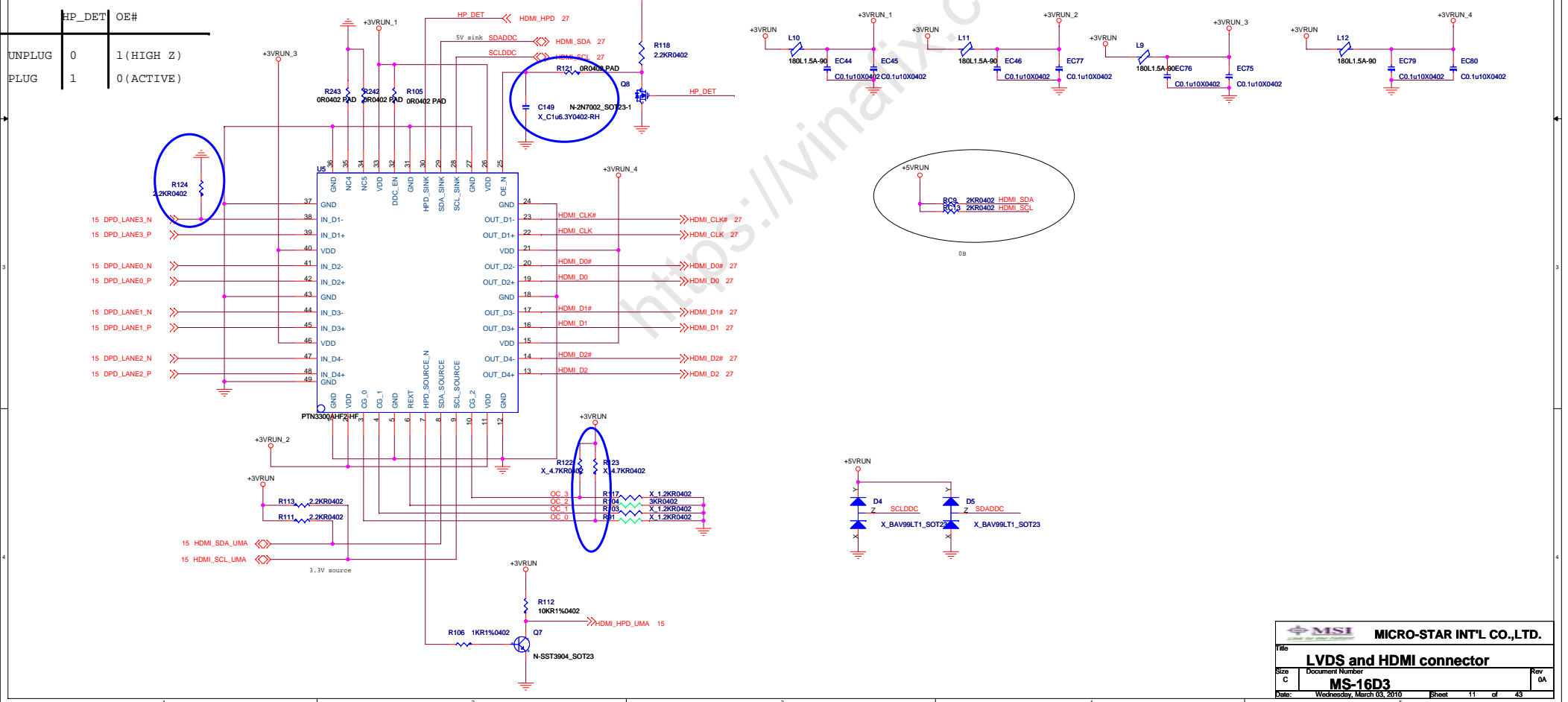
# SODIMM#B



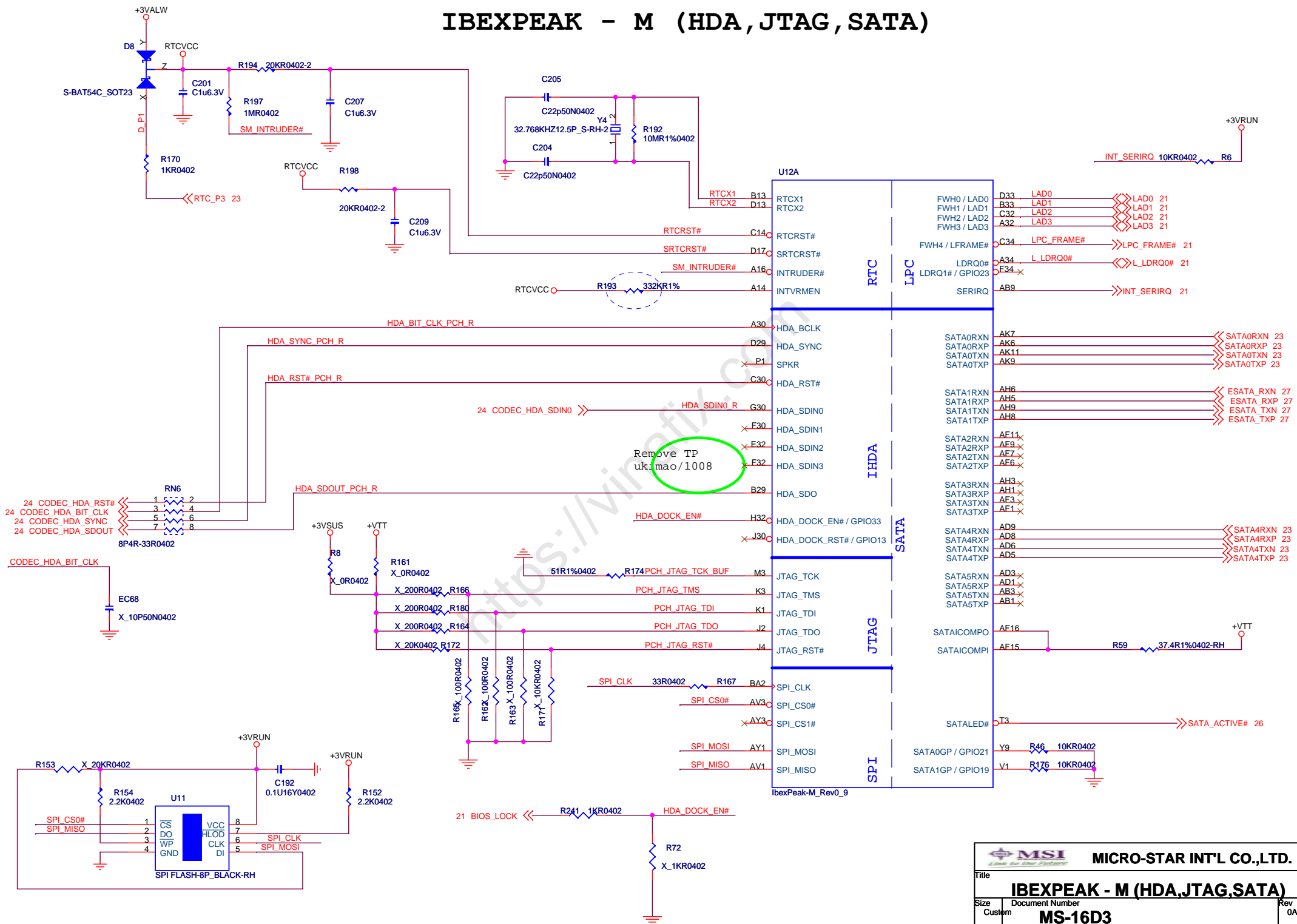
# LVDS connector



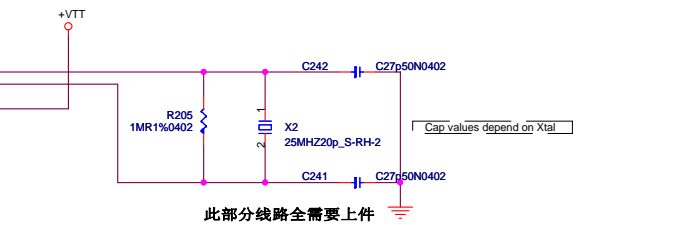
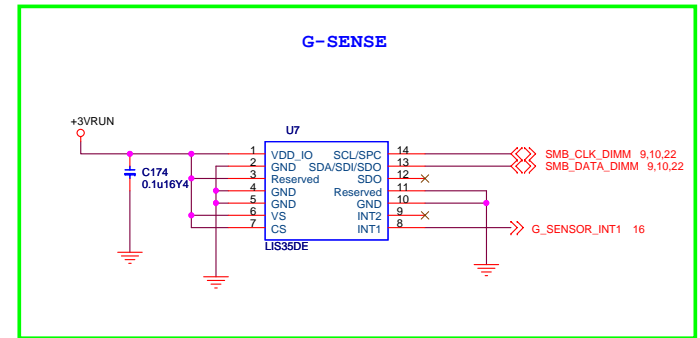
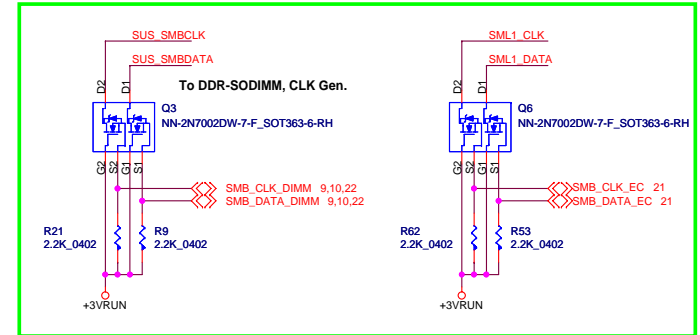
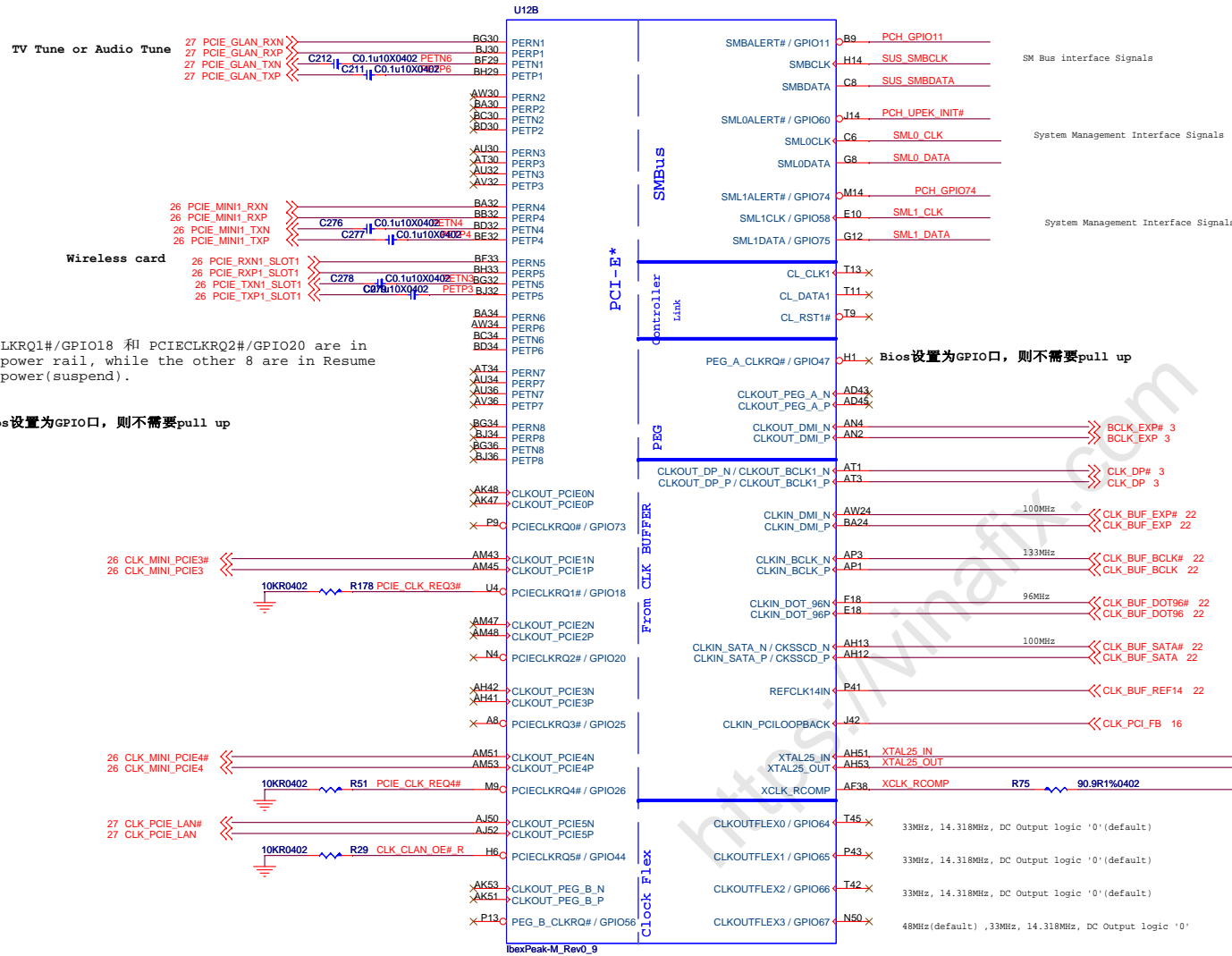
## HDMI Switch



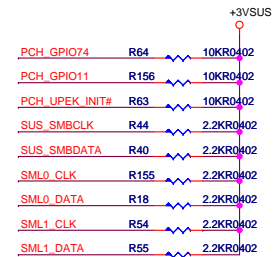
# IBEXPEAK - M (HDA, JTAG, SATA)



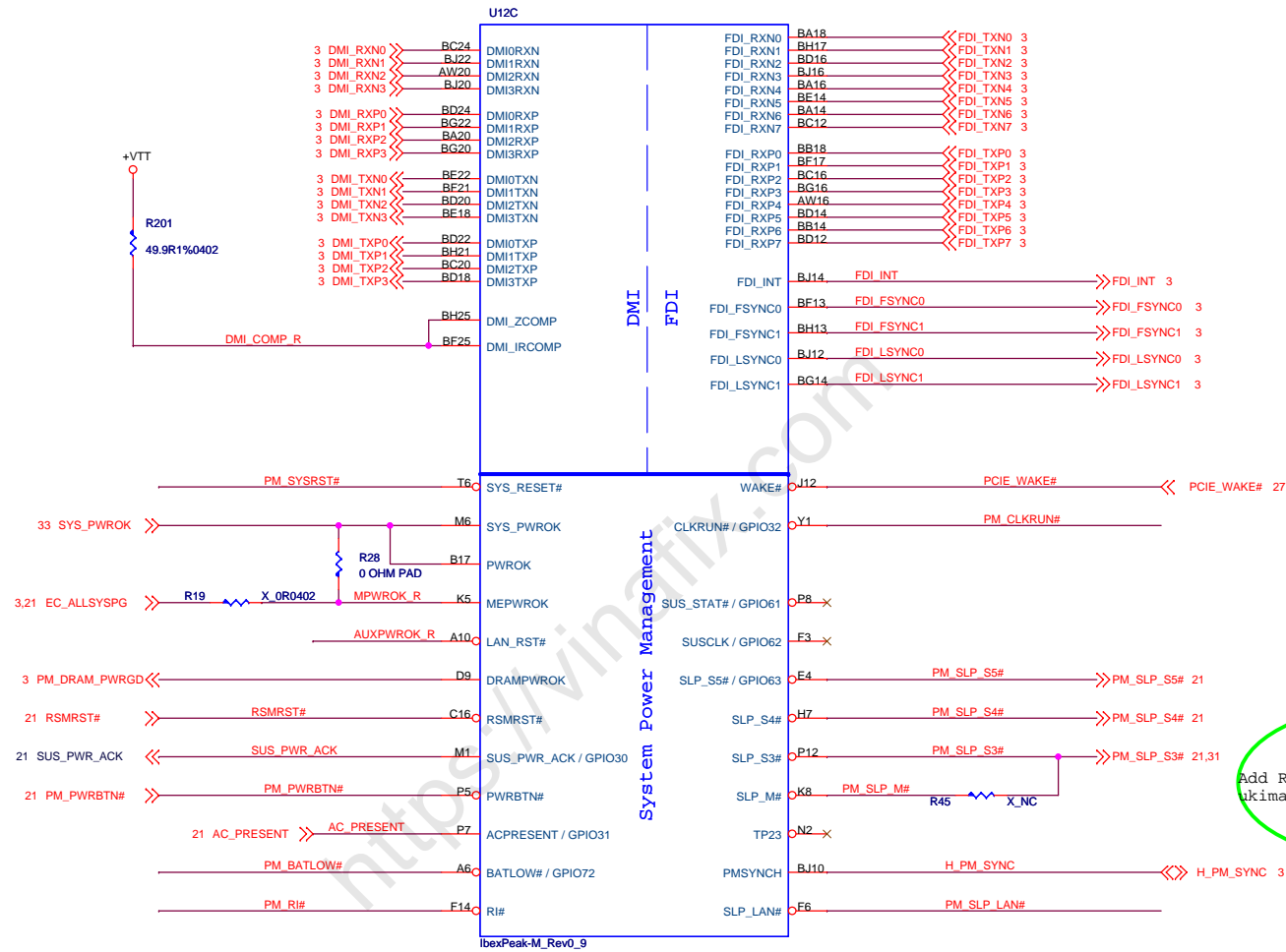
# IBEXPEAK - M (PCI-E, SMBUS, CLK)



Bios设置为GPIO口, 则不需要pull up



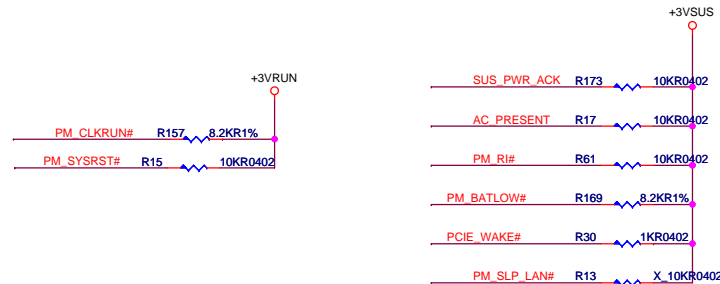
# IBEXPEAK - M (DMI, FDI, GPIO)



Add R3400 for intel suggestion  
ukimao/1108

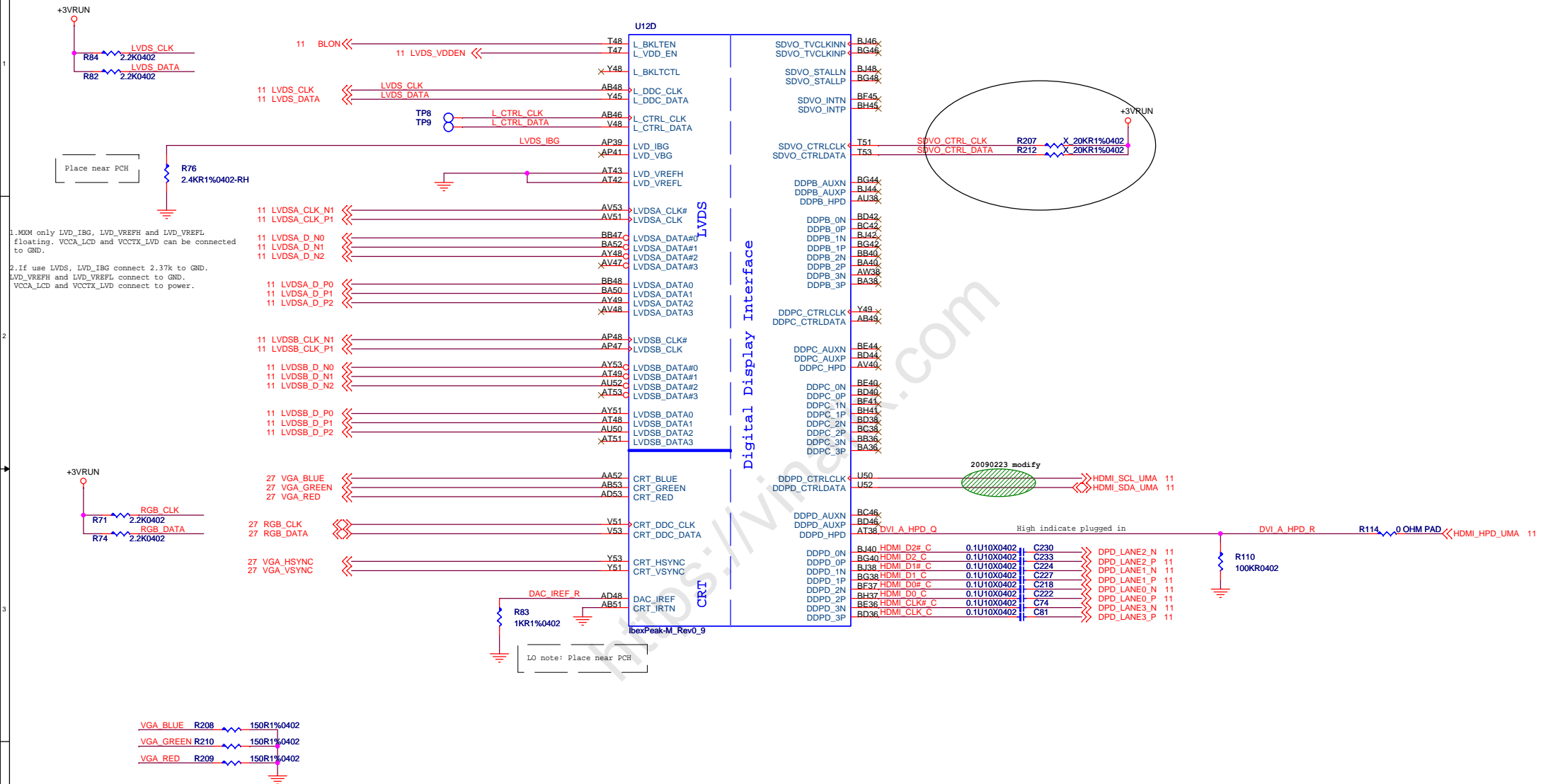
PULL LOW FOR EXTERNAL LAN

If integrated LAN is not used:  
LAN\_RST# to GND via an 8.2k to 10kohm pull-down resistor.  
connector the VccLAN pins on PCH directly to GND.

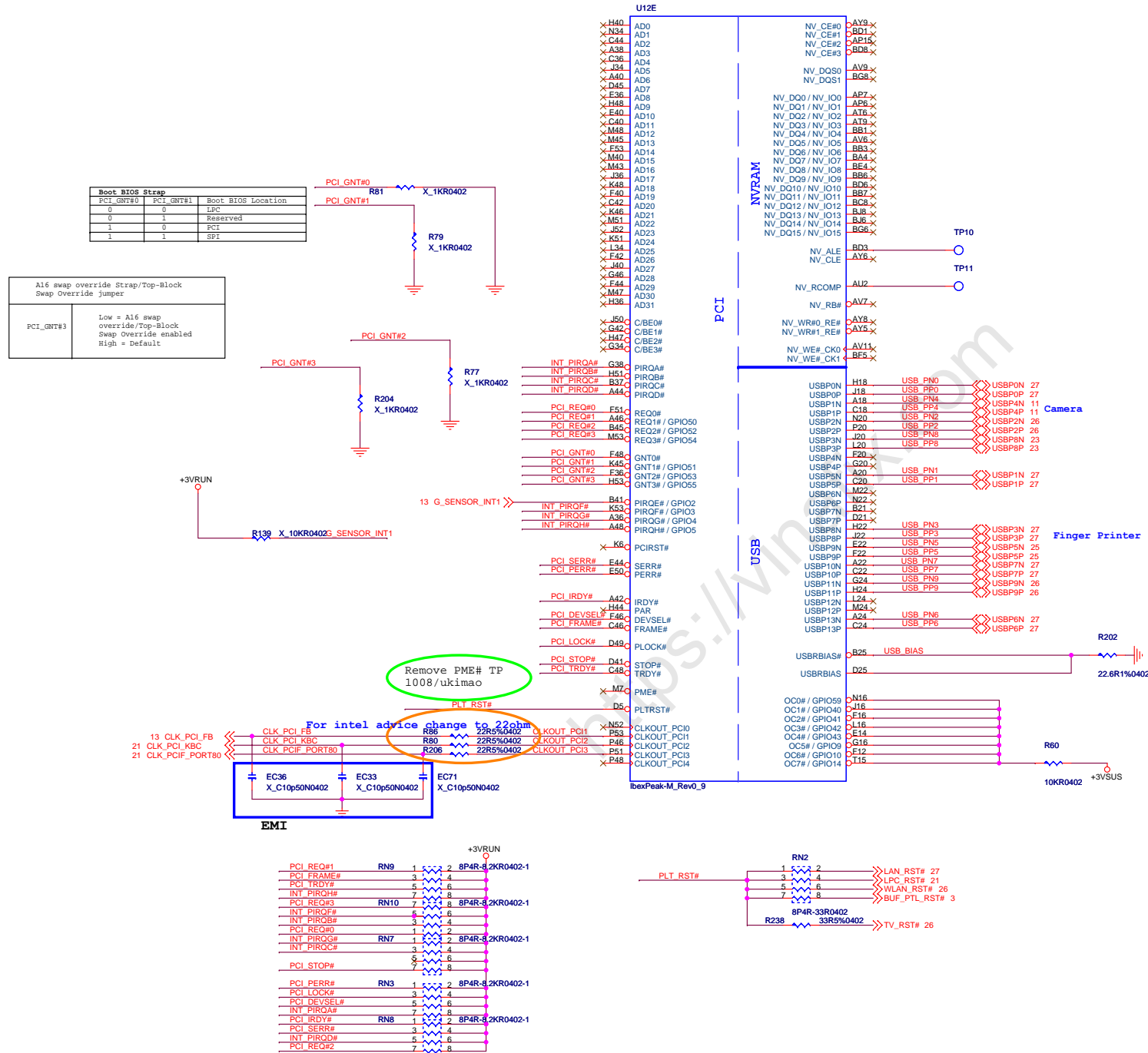




# IBEXPEAK - M (LVDS,DDI)

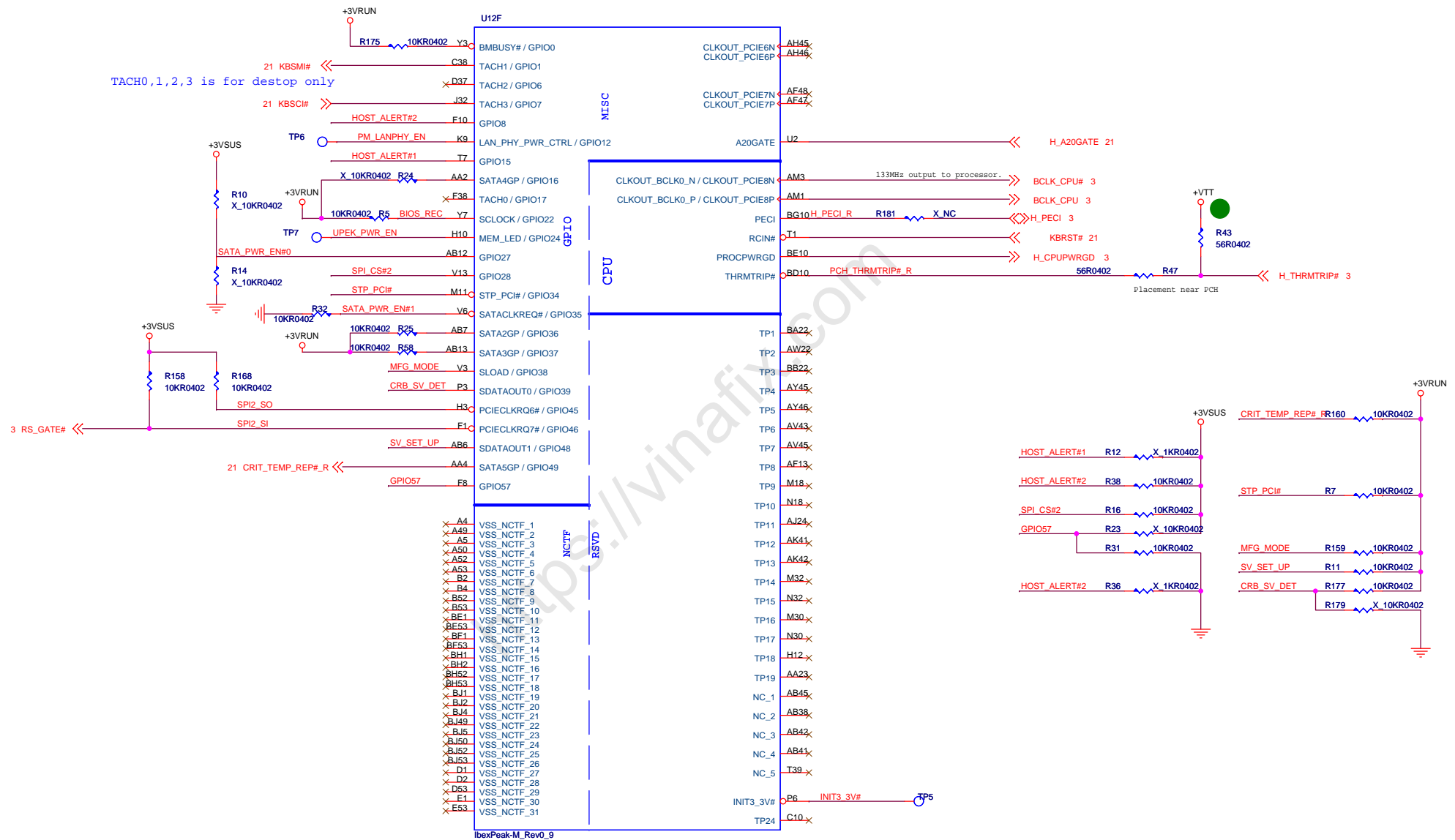


# IBEXPEAK - M (PCI,USB,NVRAM)

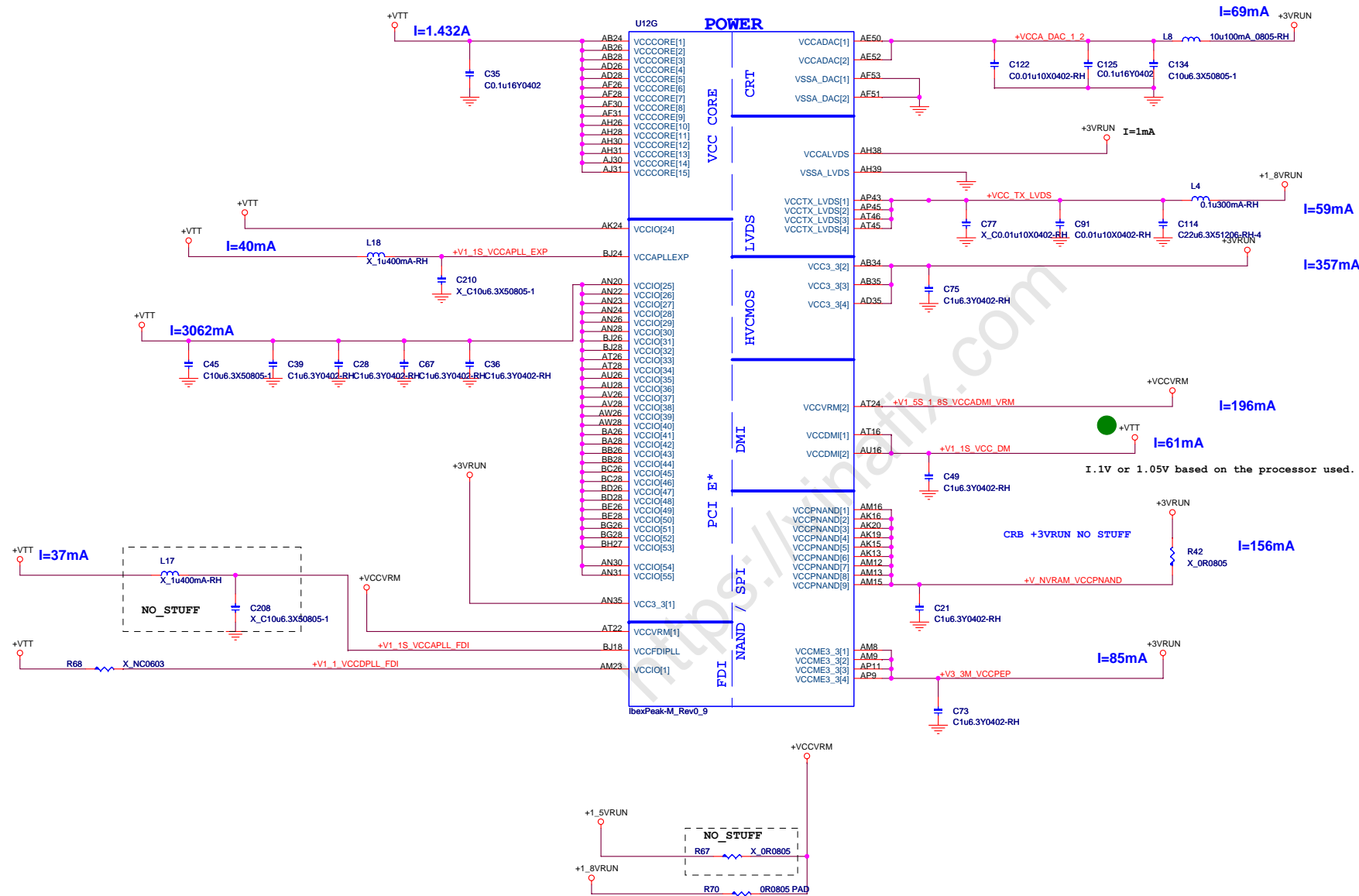


J3 - BBS STRAP  
DEFAULT: 1-X

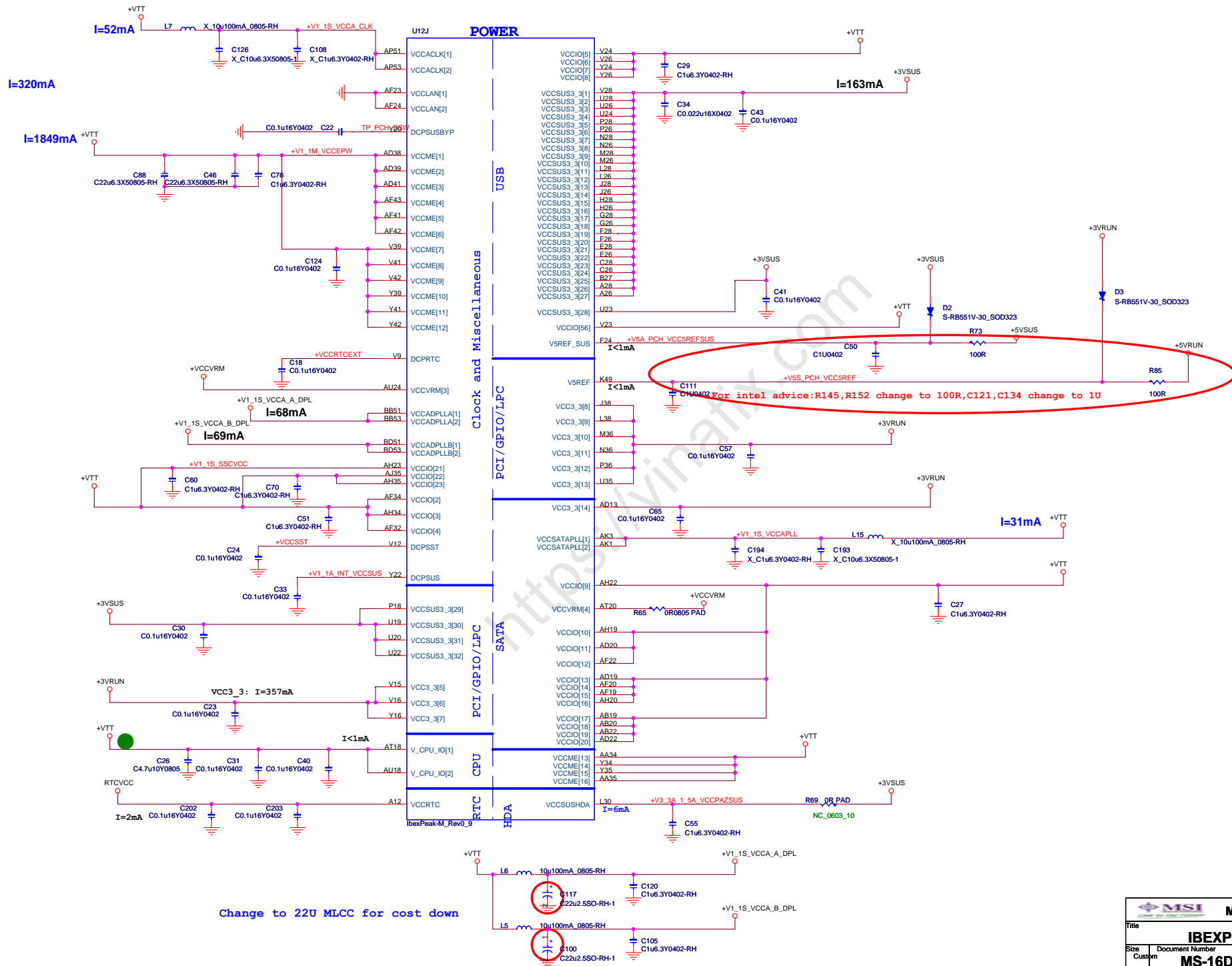
**IBEXPEAK - M (GPIO,VSS\_NCTF,RSVD)**



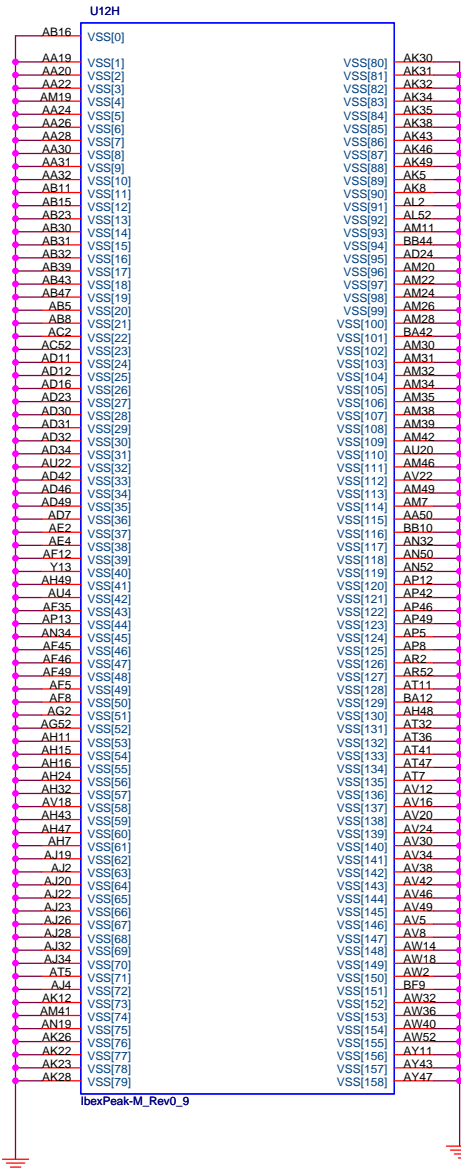
# IBEXPEAK - M (POWER)



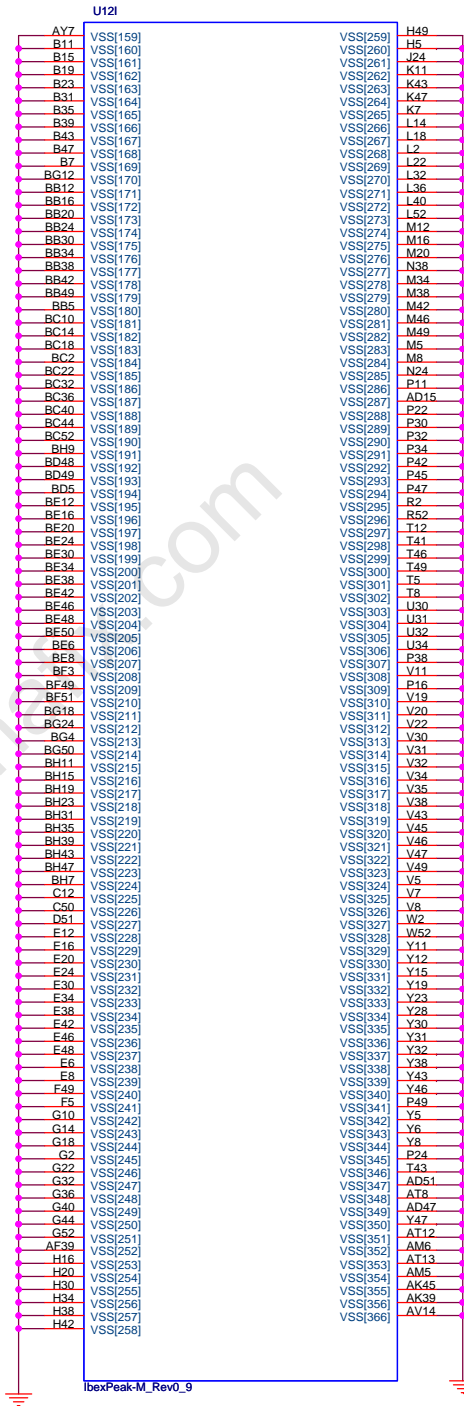
The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

**IBEXPEAK - M (POWER)**


# IBEXPEAK - M (GND)

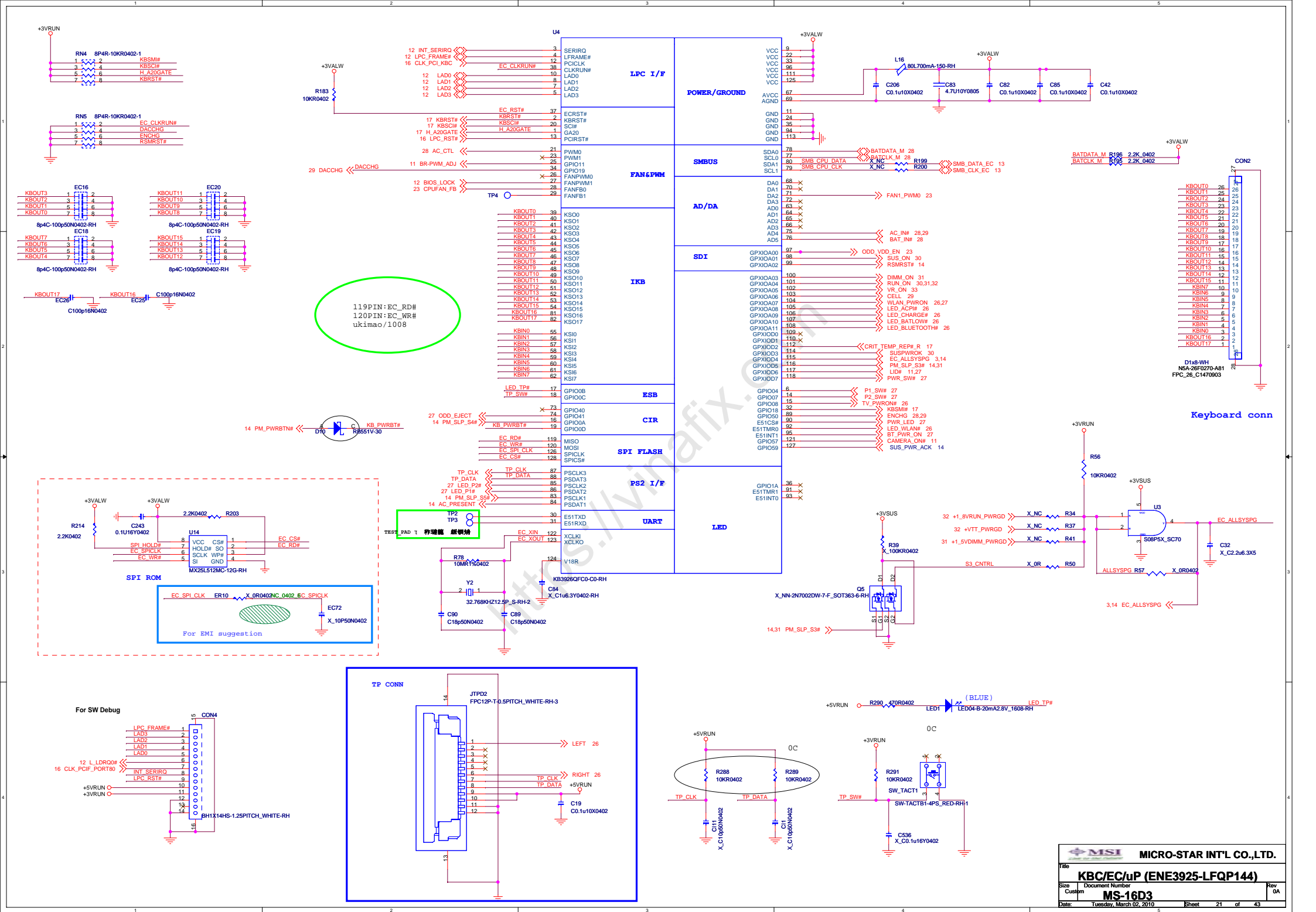


IbexPeak-M\_Rev0\_9



IbexPeak-M\_Rev0\_9

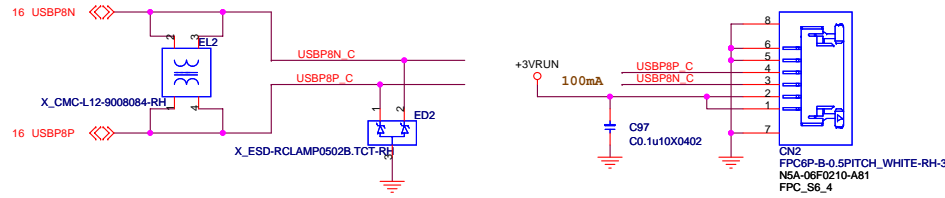
		MICRO-STAR INT'L CO.,LTD.	
Title			
IBEXPEAK - M (GND)			
Size	Document Number		Rev
Custom	MS-16D3		0A
Date:	Thursday, November 26, 2009	Sheet	20 of 43



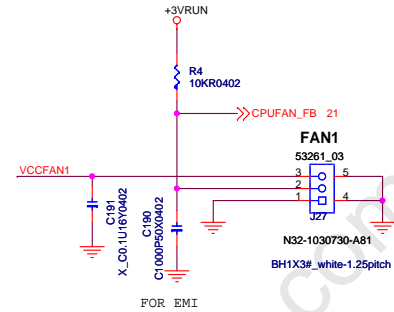
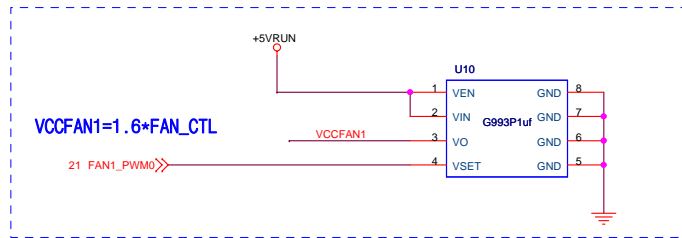




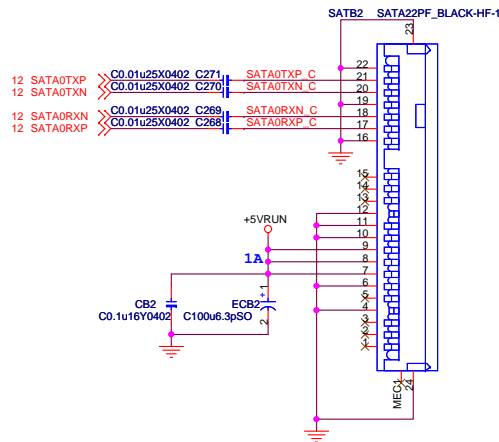
## FINGER PRINT



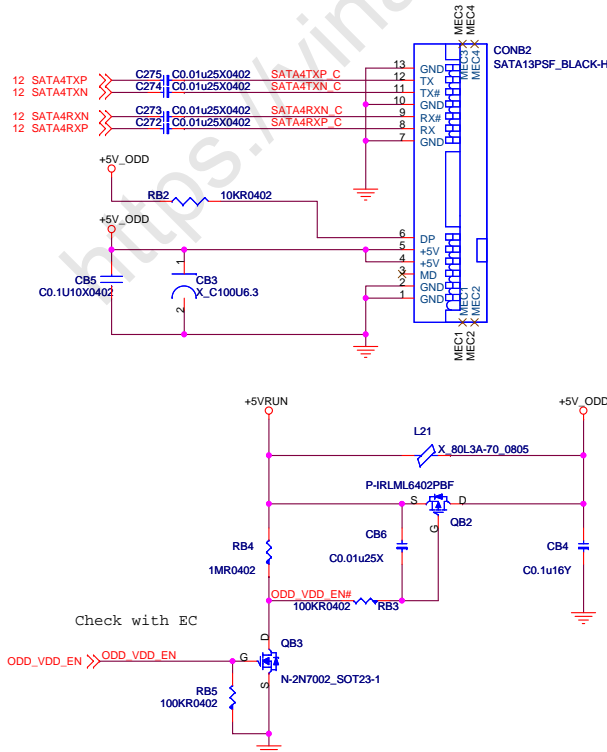
## CPU FAN CTRL



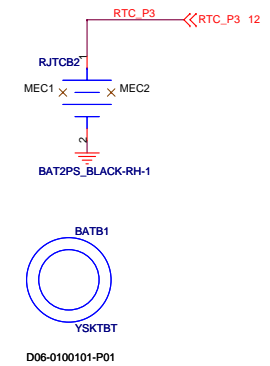
## SATA HDD Connector



## SATA ODD Connector



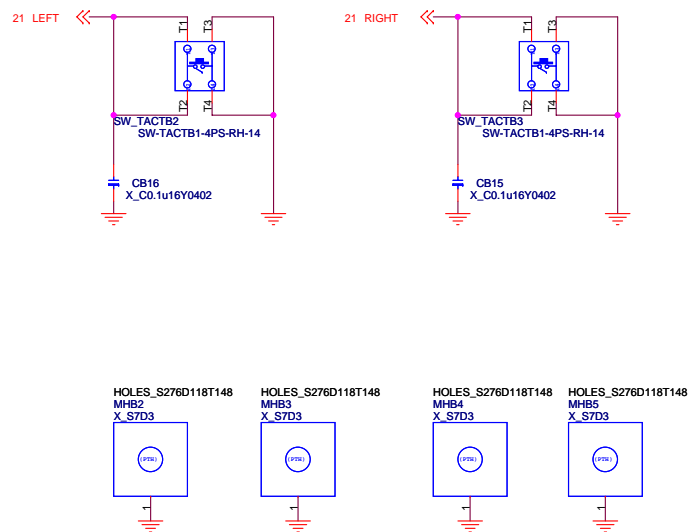
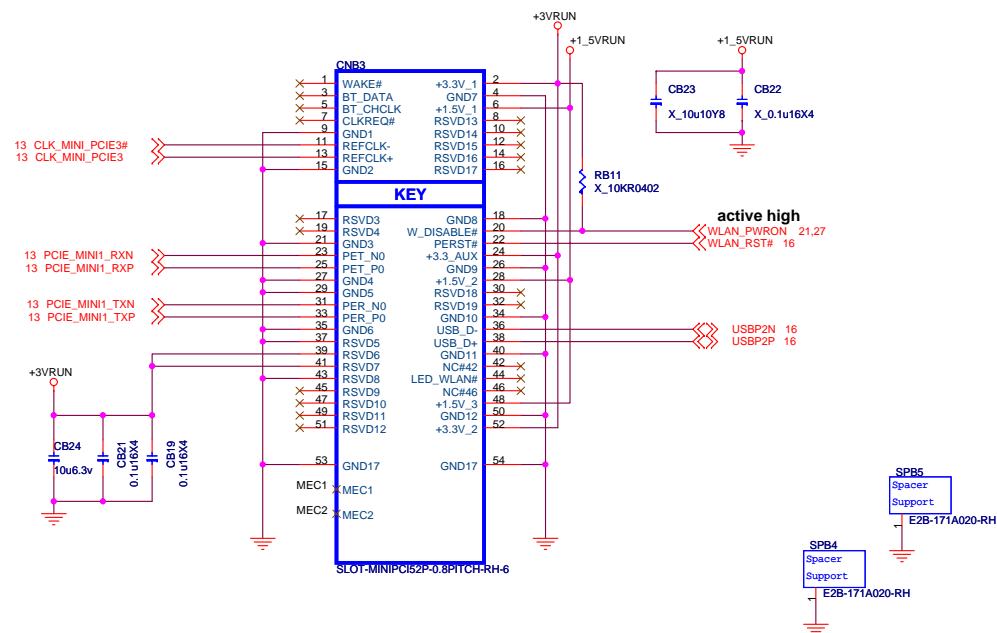
## RTC Connector



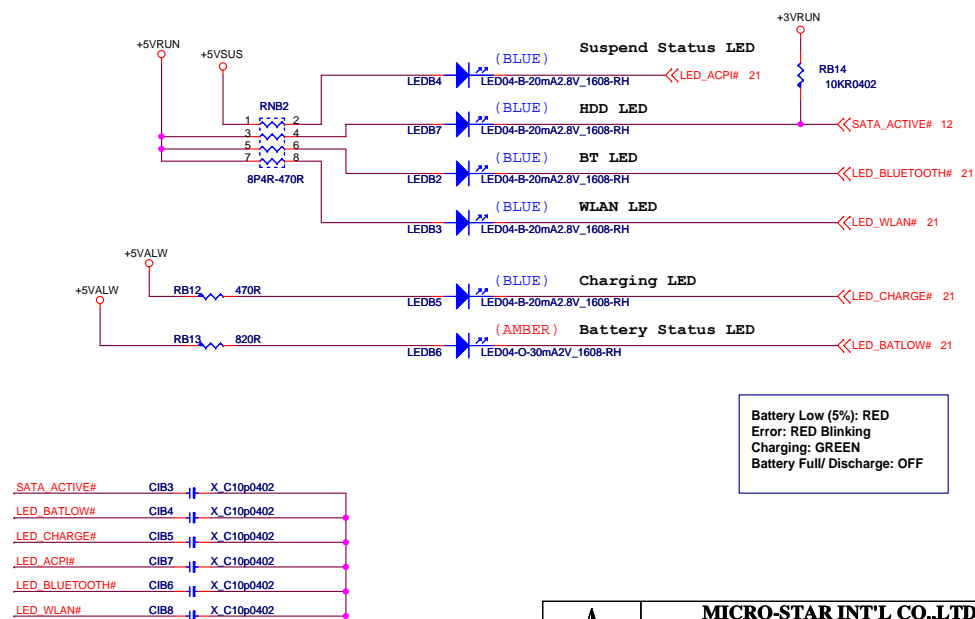
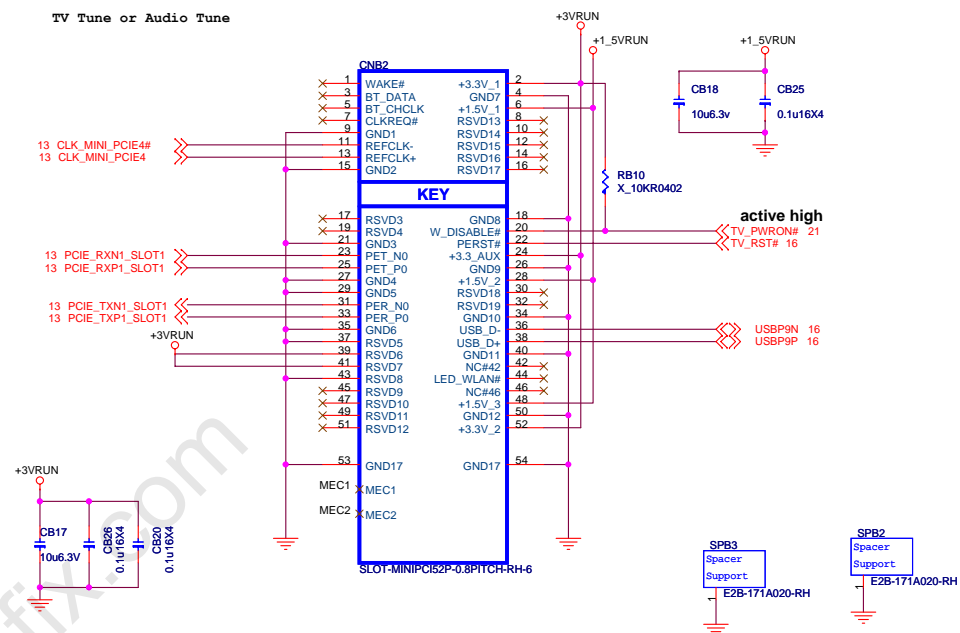




## MINI PCIE Connector



## MINI PCIE Connector



For EMI



**MICRO-STAR INT'L CO.,LTD**

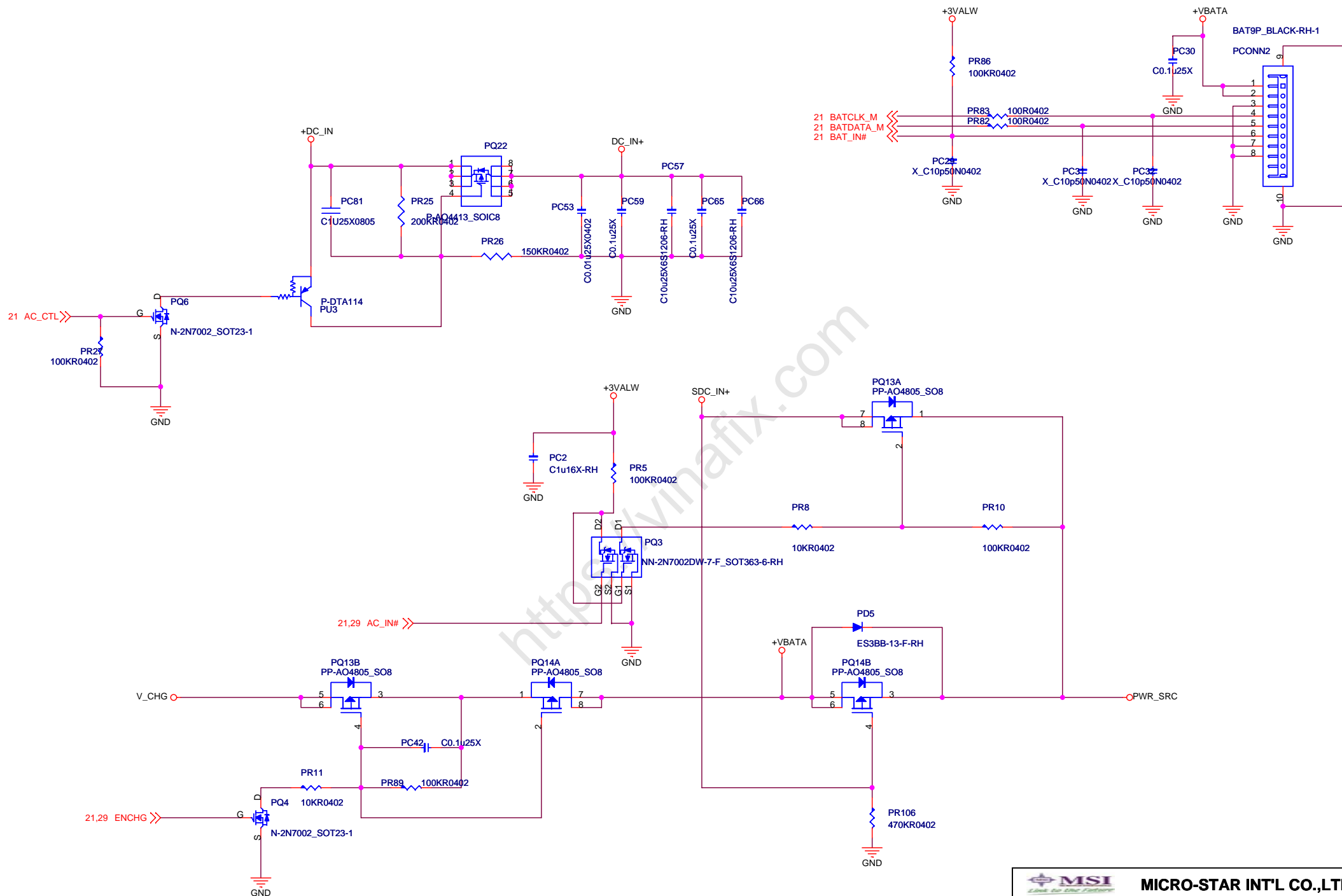
**MS-16D3**

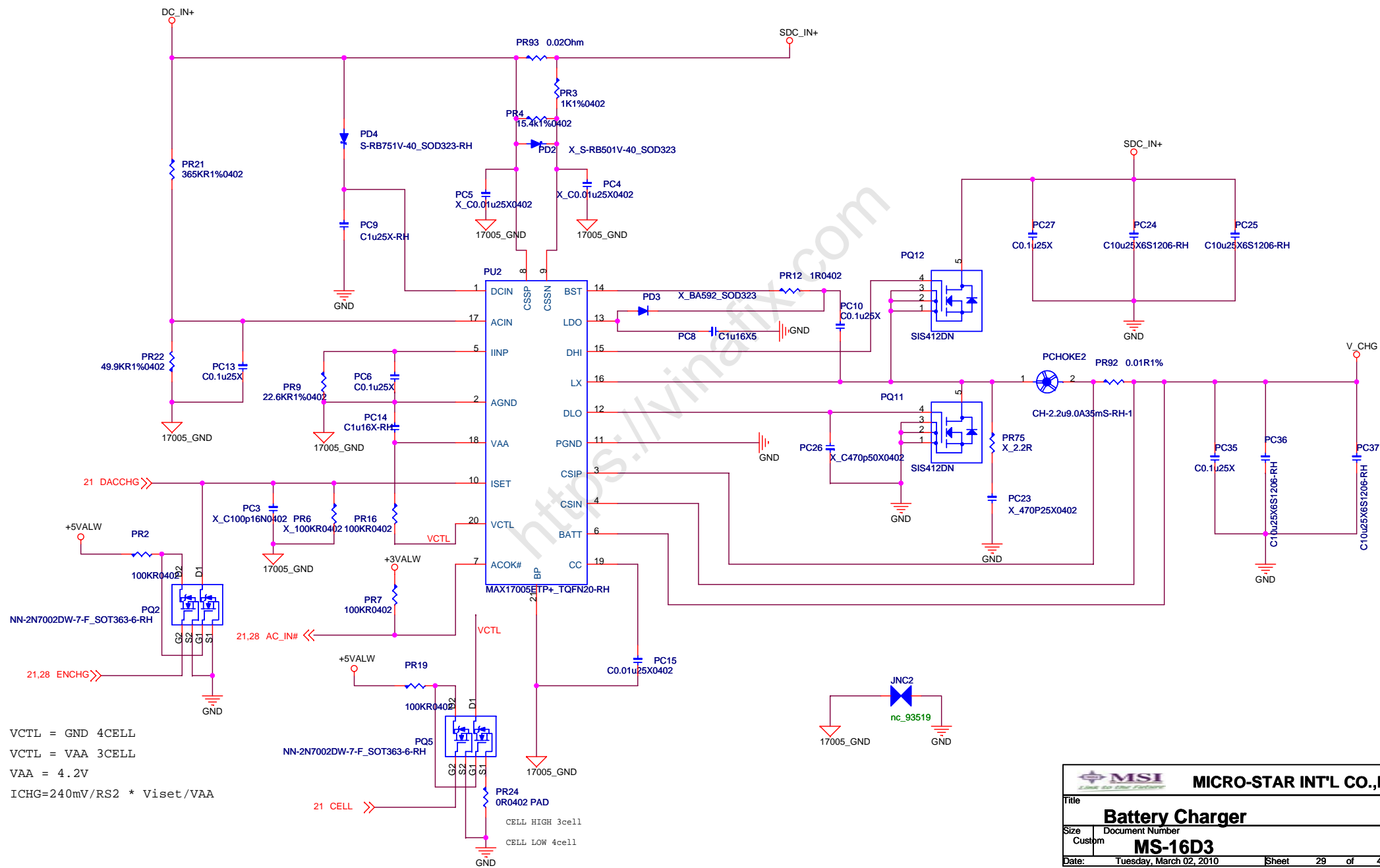
Size	Document Description
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Custom	<b>MINI PCIE / TP / LED</b>
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Date: Tuesday, March 02, 2010

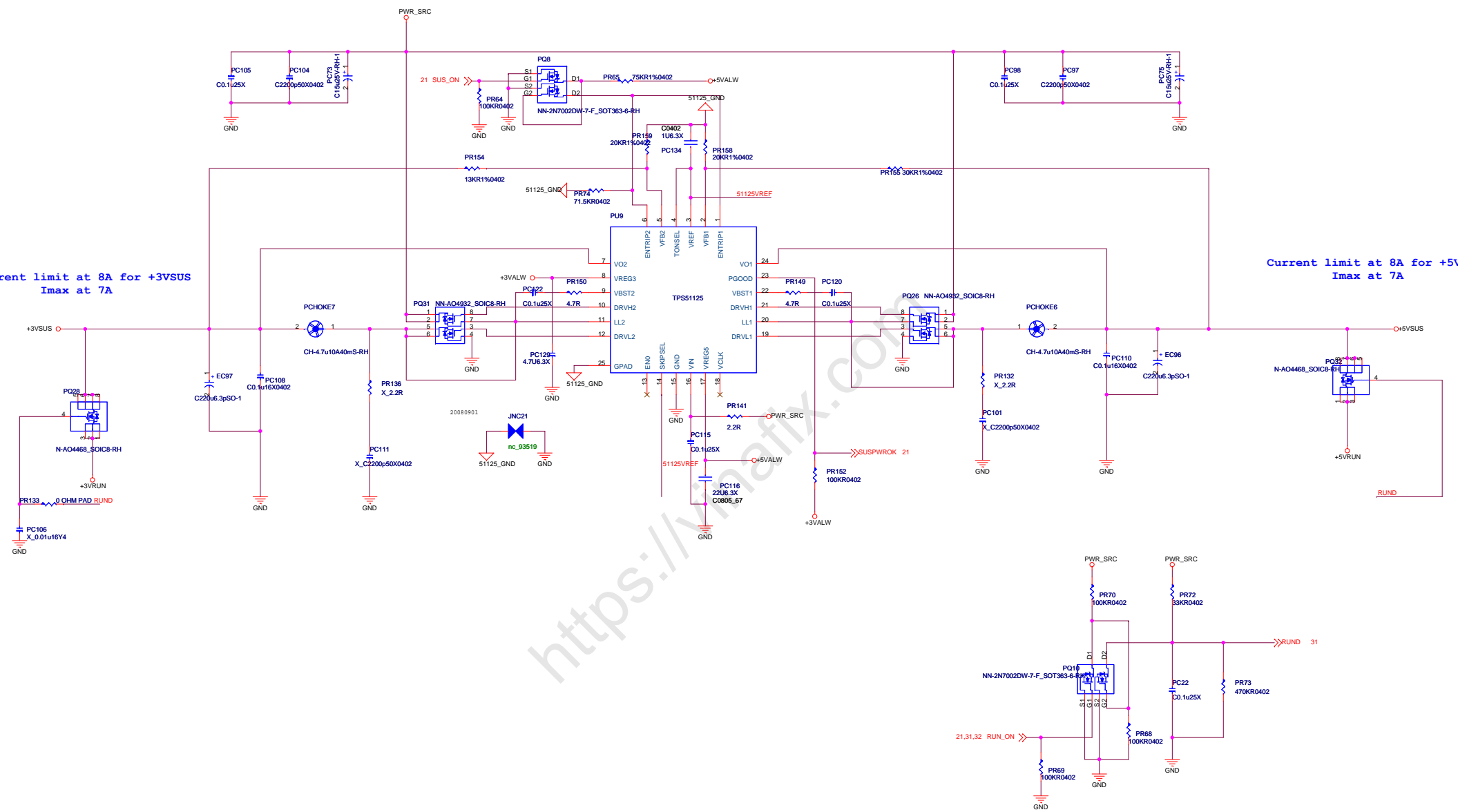
Rev	0A
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Current limit at 8A for +3VSUS  
Imax at 7A

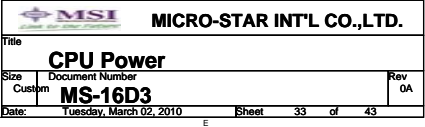
Current limit at 8A for +5VSUS  
Imax at 7A



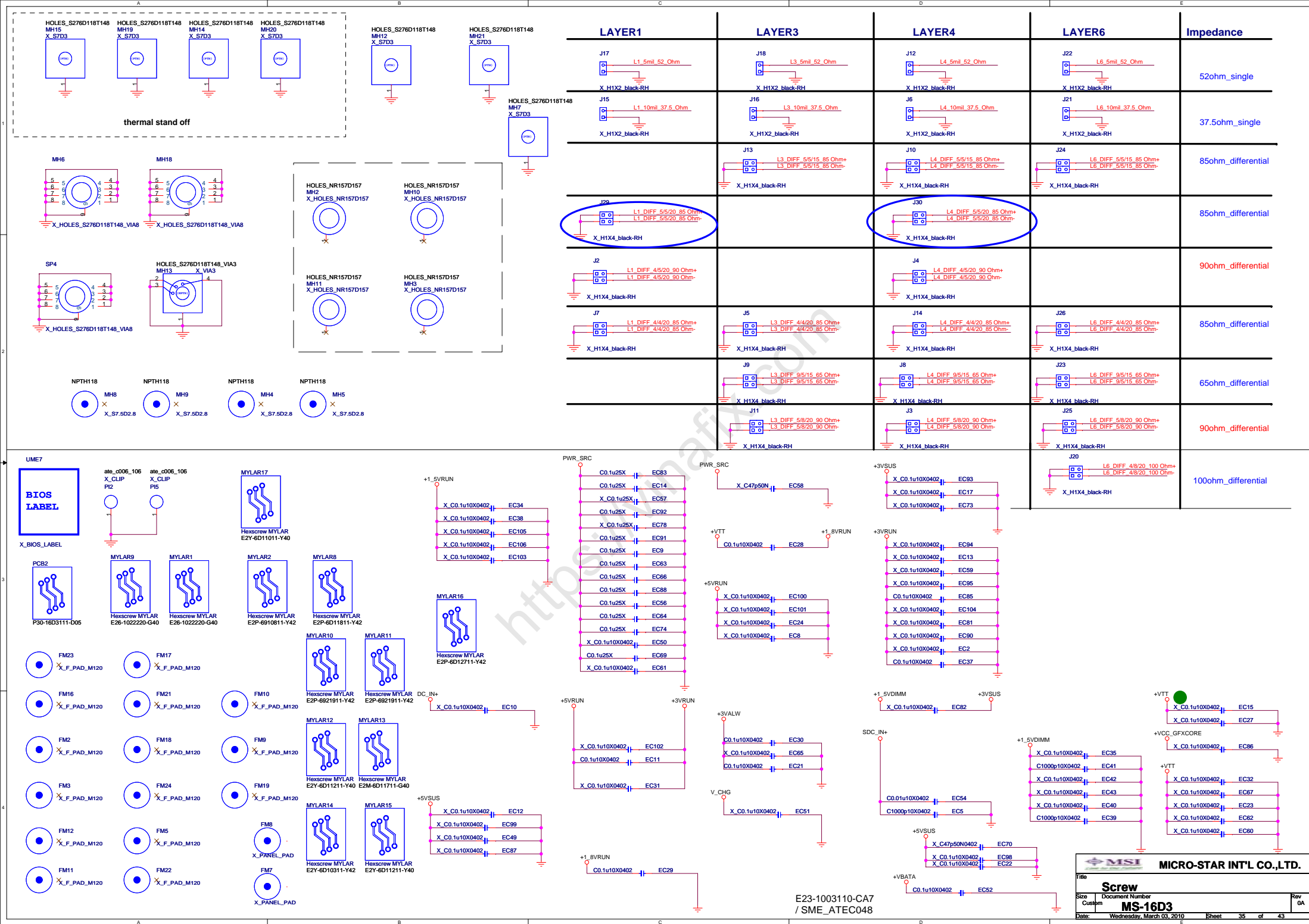




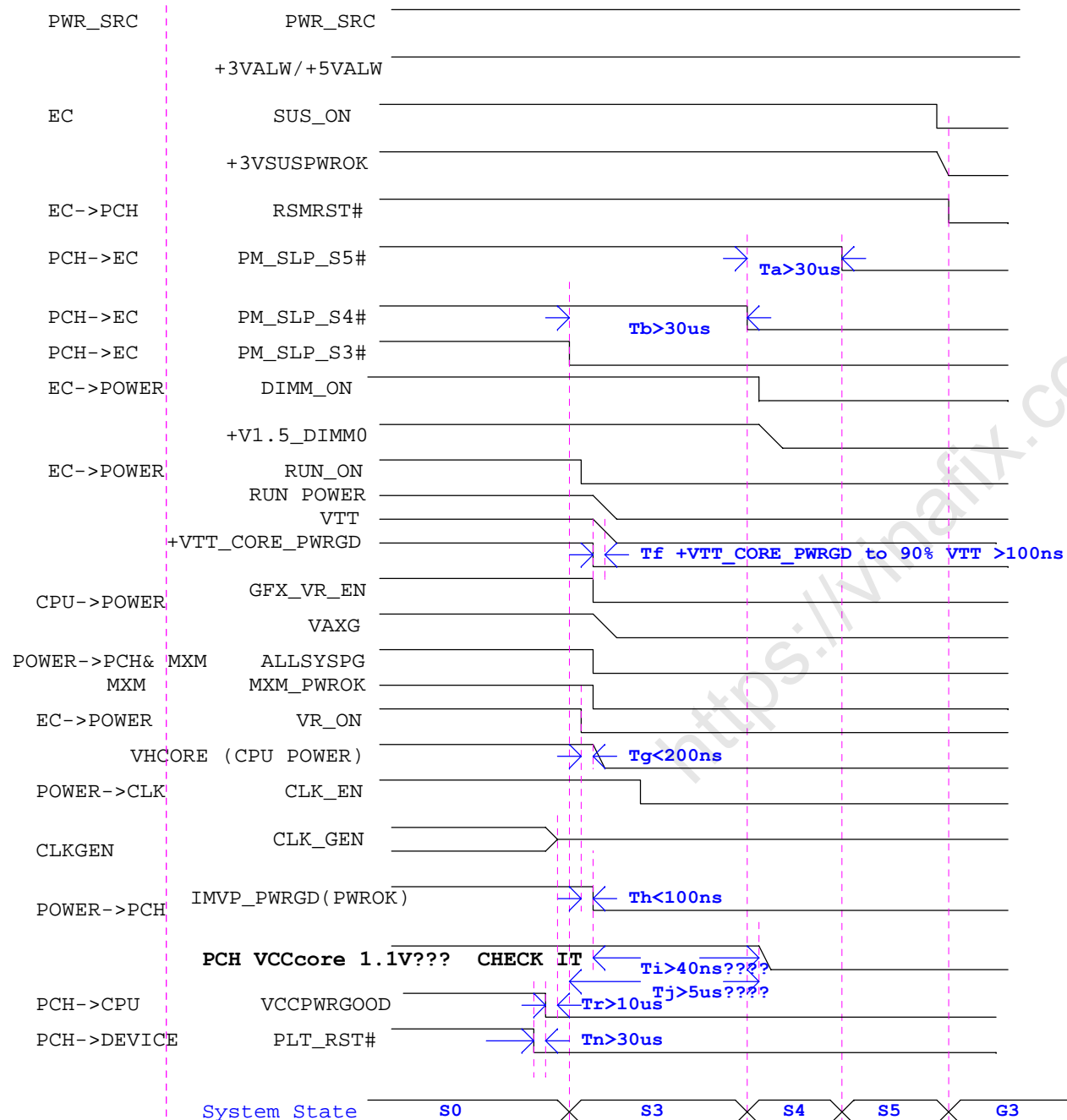




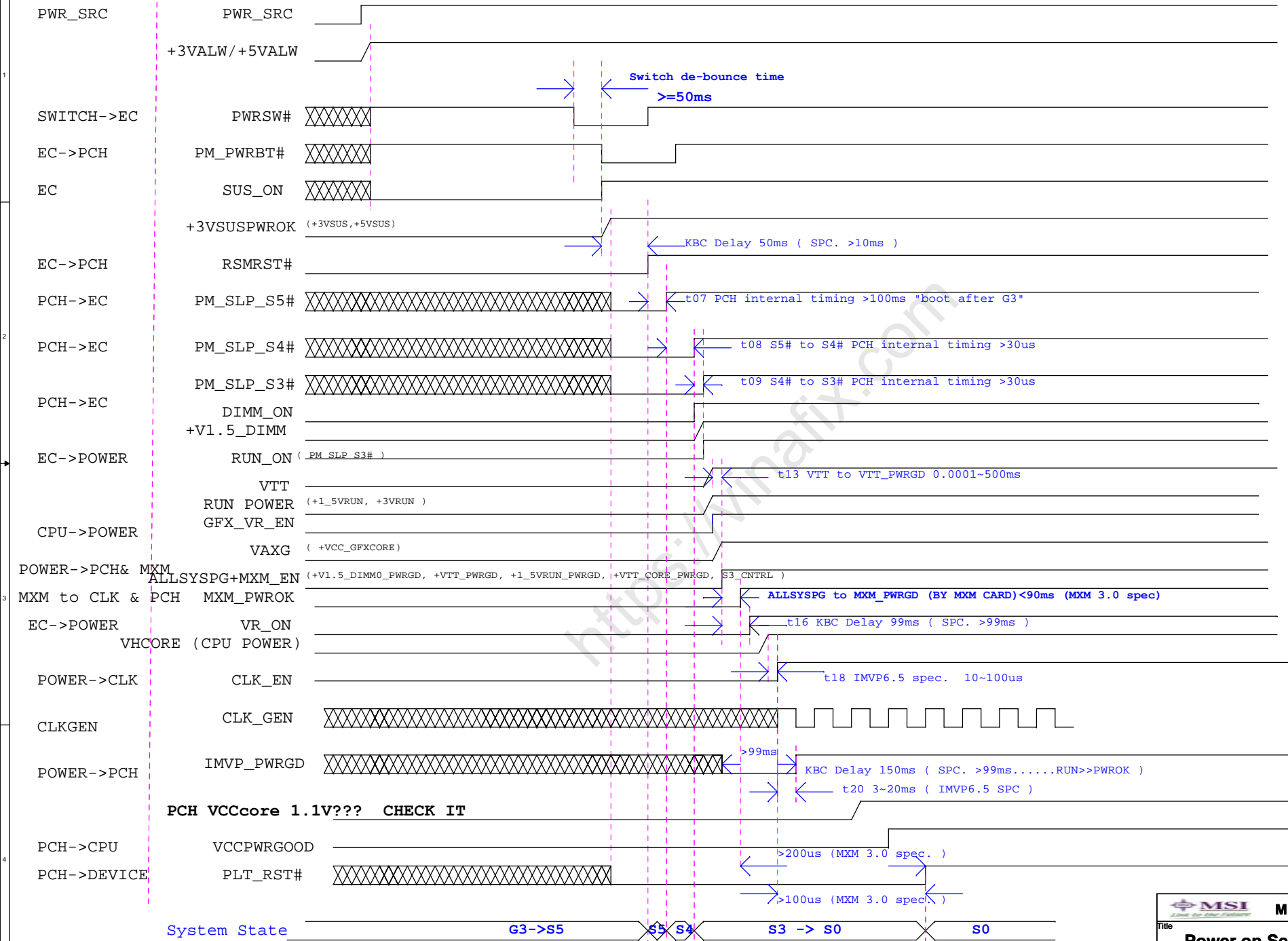




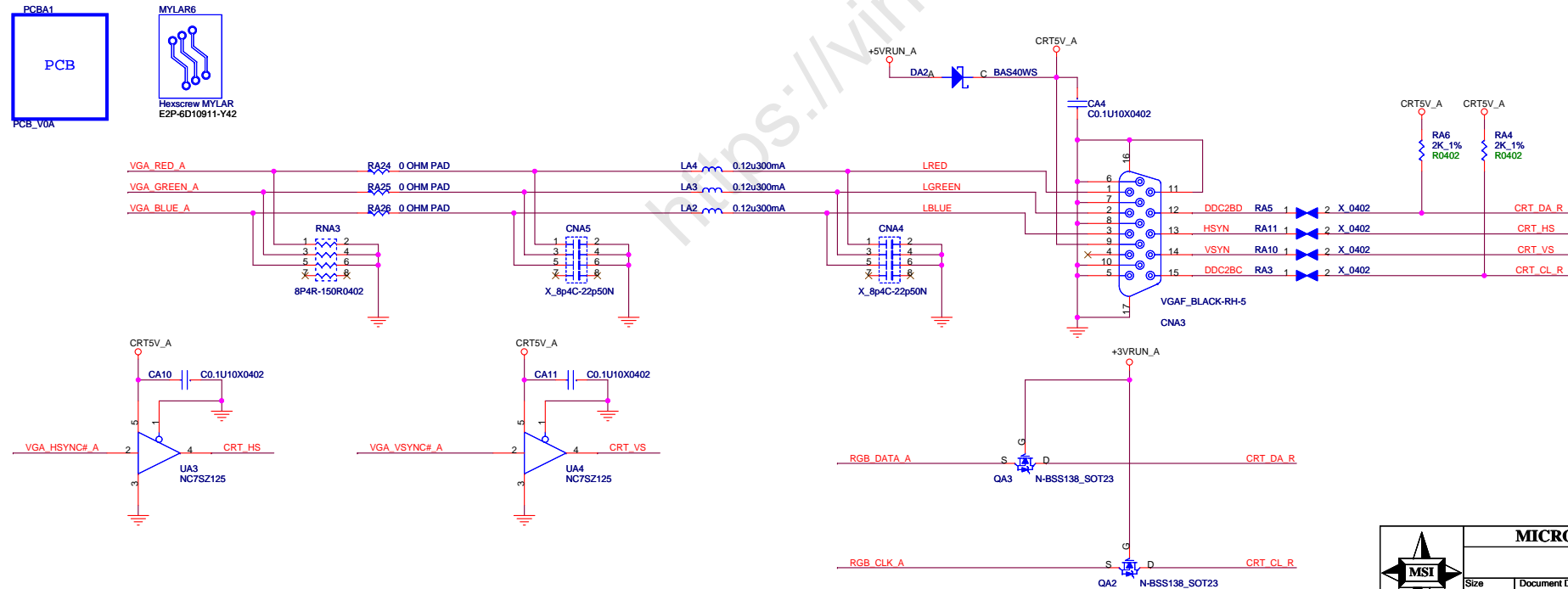
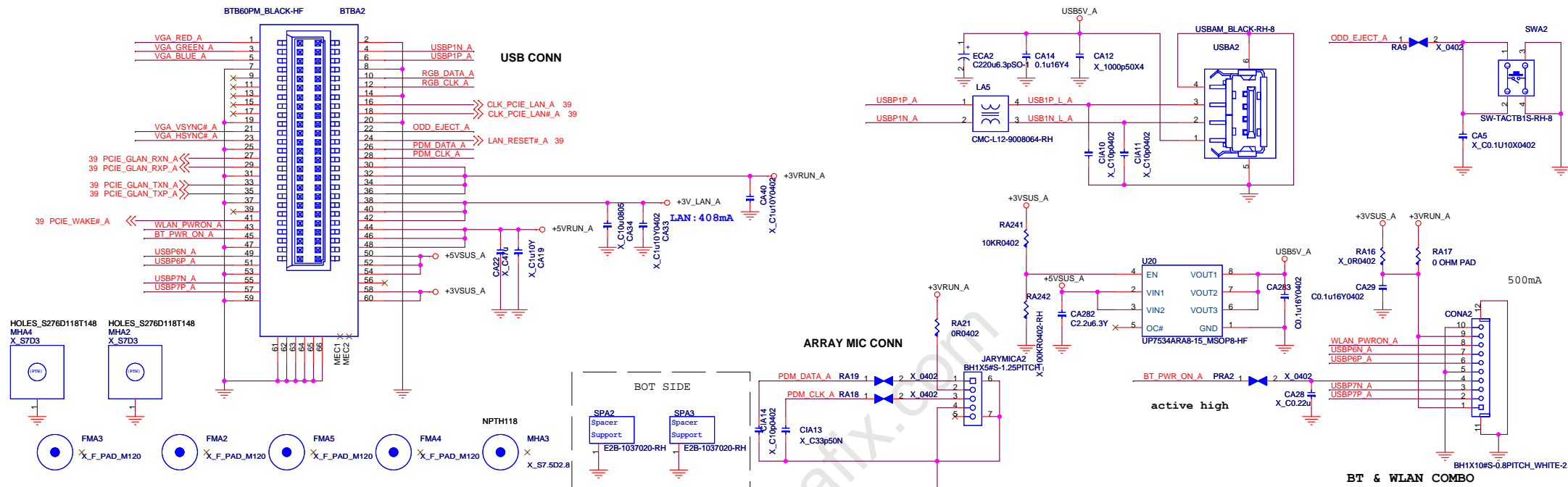
# Power down Sequence DC mode S0 to G3



# Calpella System Power on Sequence DC mode



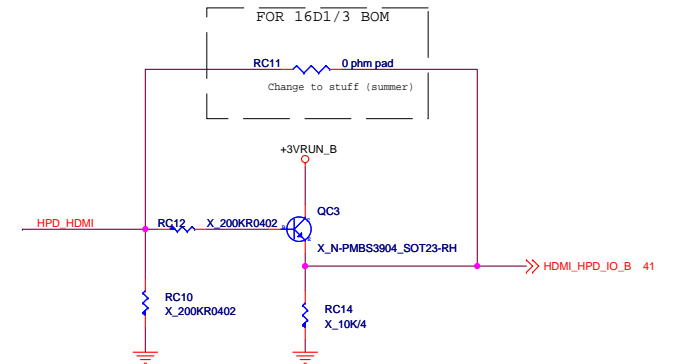
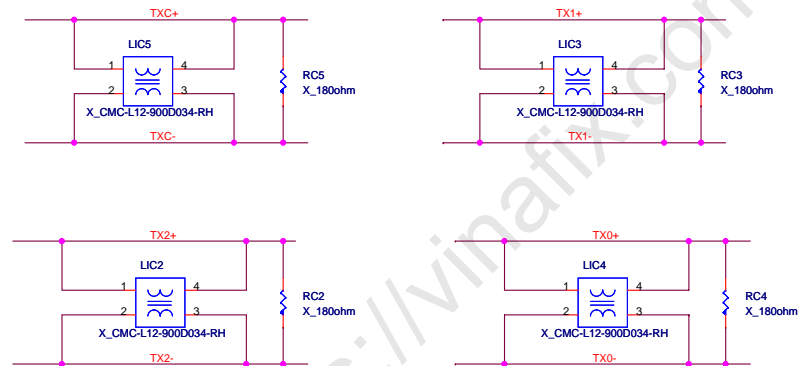
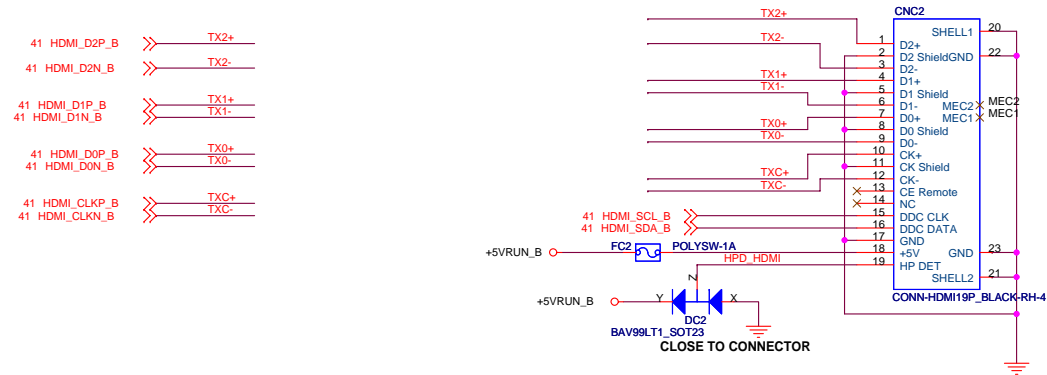
**60PIN BTB I/O Connector(VGA, USBX1, LAN,BT,ARRAY MIC)**



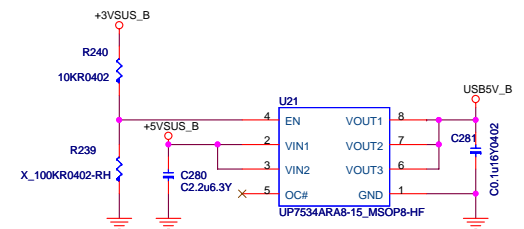
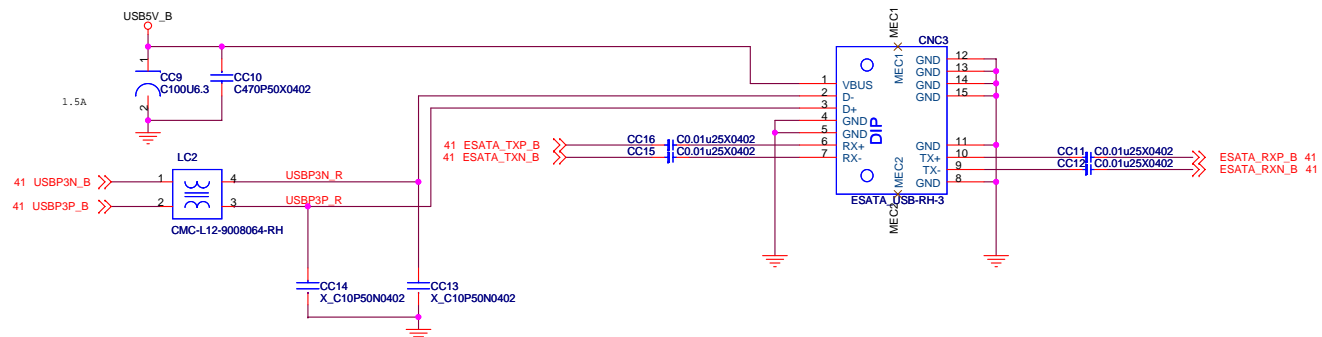




## HDMI



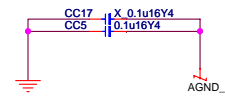
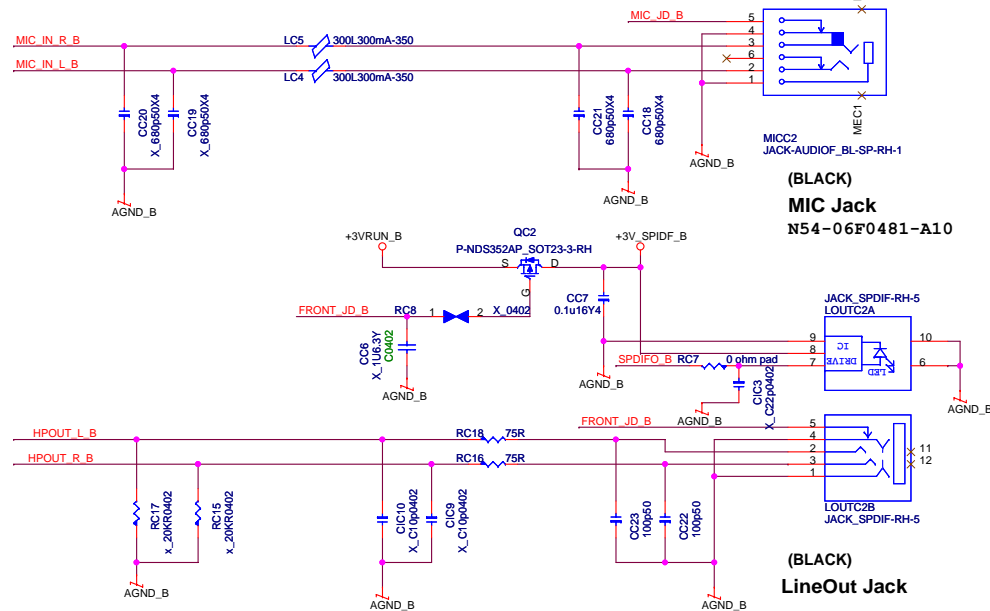
**ESATA**



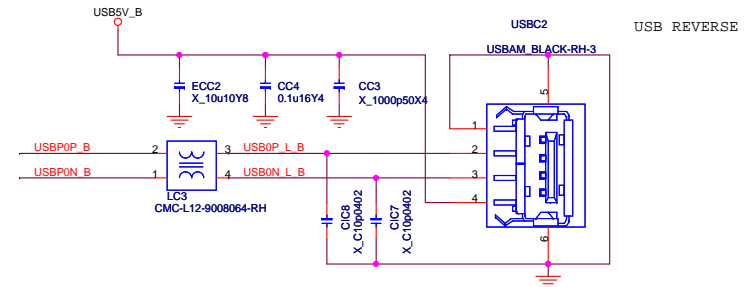
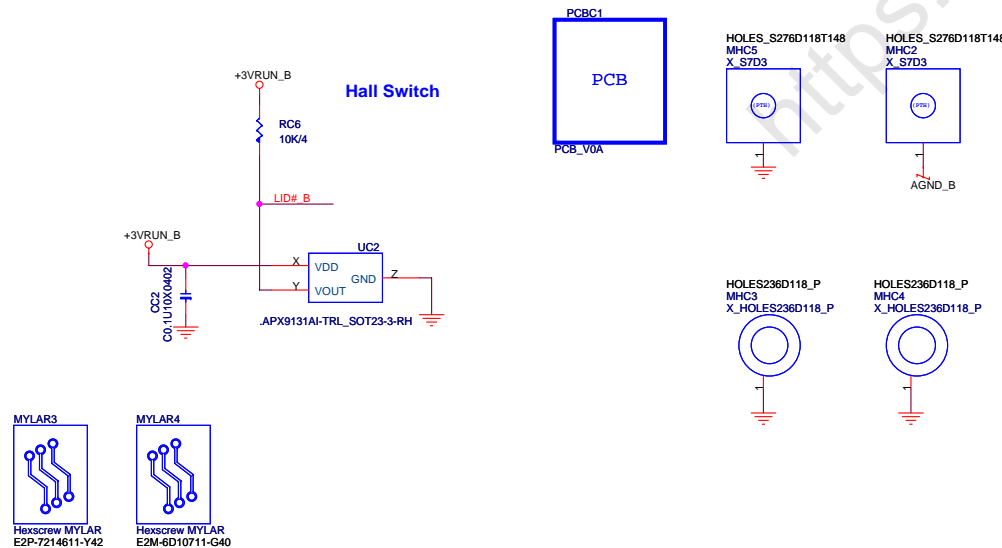
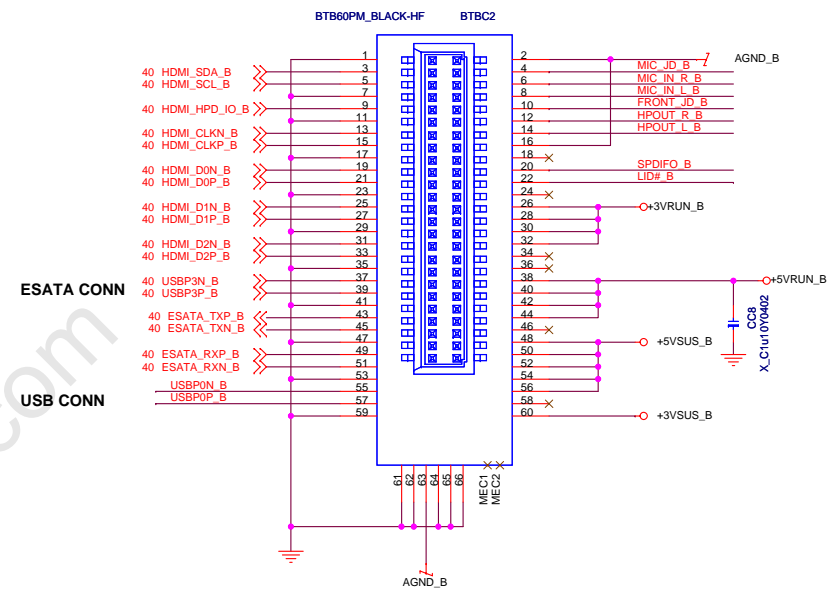
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**MS-16D3B**

Size Custom	Document Description <b>HDMI/ ESATA</b>	Rev 0A
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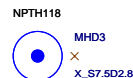
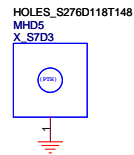
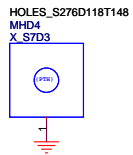
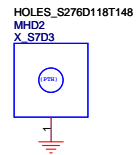
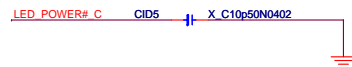
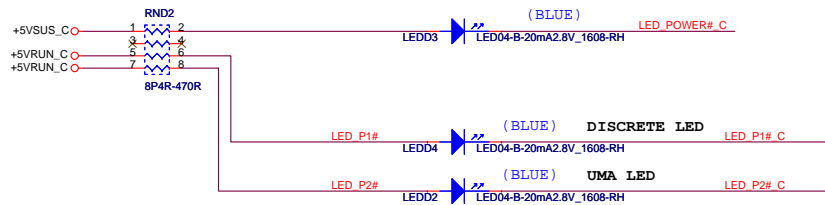
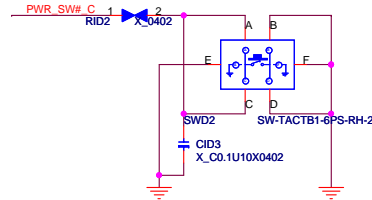
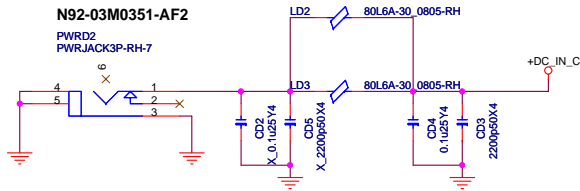


## 60PIN BTB I/O Connector(HDMI,ESATA, Audio) USBX1)

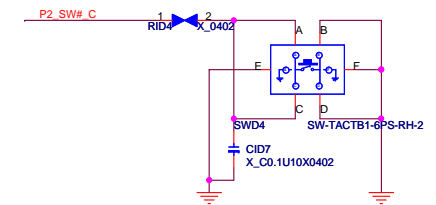
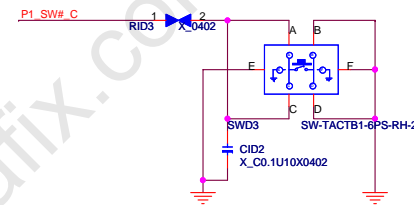
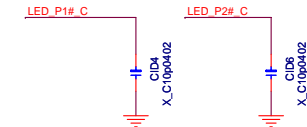
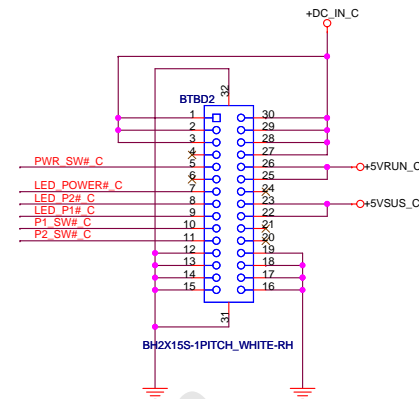


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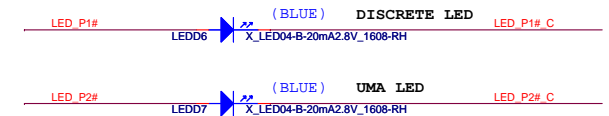
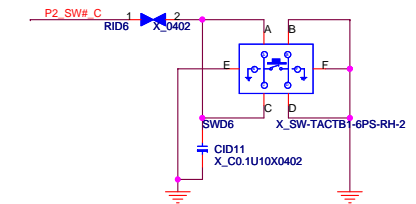
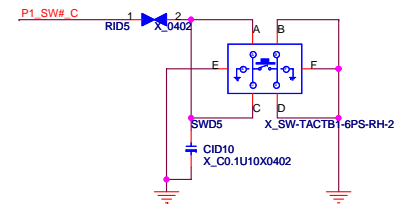
PWRD2  
PWRJACK3P-RH-7



## 30PIN BTB I/O Connector( AC IN ,Switch(Power ,UMA,Discrete )



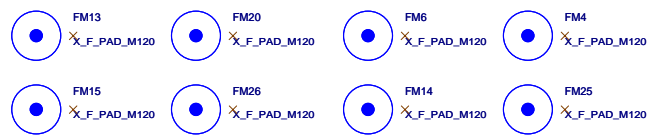
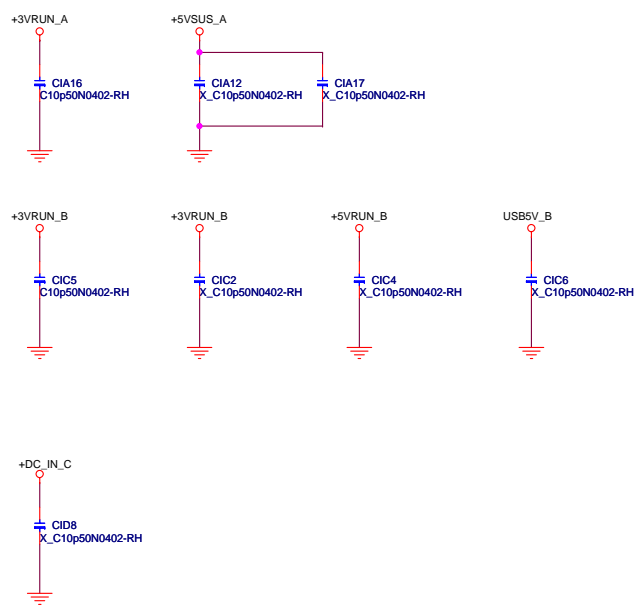
FOR 16D1 WLAN&P1 SWITCH



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Custom	DCIN/SW/CONN	0A
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